■ INTRODUCTION

RW1073 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It is capable of displaying 1, 2, or 4-lines with 5×8 or 6×8 dots format.

■ FUNCTIONS

- Character type dot matrix LCD driver & controller
- Internal driver: 34 common and 60 segment signal output
- Easy interface with 4-bit or 8-bit MPU and SPI interface
- Clock synchronized serial Interface
- 5×8 or 6x8 dot matrix possible
- Extension driver interface possible
- Bidirectional shift function
- All character reverse display
- Display shift per line
- Various instruction functions
- Automatic power on reset
- Voltage converter for LCD drive voltage: 8V max (2 times/ 3 times)

■ FEATURES

- Internal Memory
  - Character Generator ROM (CGROM): 9600 bits. (240 characters × 5 × 8 dot)
  - Character Generator RAM (CGRAM): 64×8 bits. (8 characters × 5 × 8 dot)
  - Segment Icon RAM (SEGRAM): 16×8 bits.(96 icons max.)
  - Display Data RAM (DDRAM): 80×8 bits. (80 characters max.)
- Low power operation
  - Power supply voltage range: 2.7 to 5.5 V (VDD)
  - LCD Drive voltage range: 3.0 to 7.2V (V0 to VSS)
- CMOS process
- Programmable duty cycle: 1/17, 1/33 (Referto Table 1.)
- Internal oscillator with an external resistor
- Low power consumption
- Bare chip available

RW1073 Revision History		
Version	**Date**	**Description**
0.0	2012/10/29	First edition

◆ Table 1 Programmable duty cycles

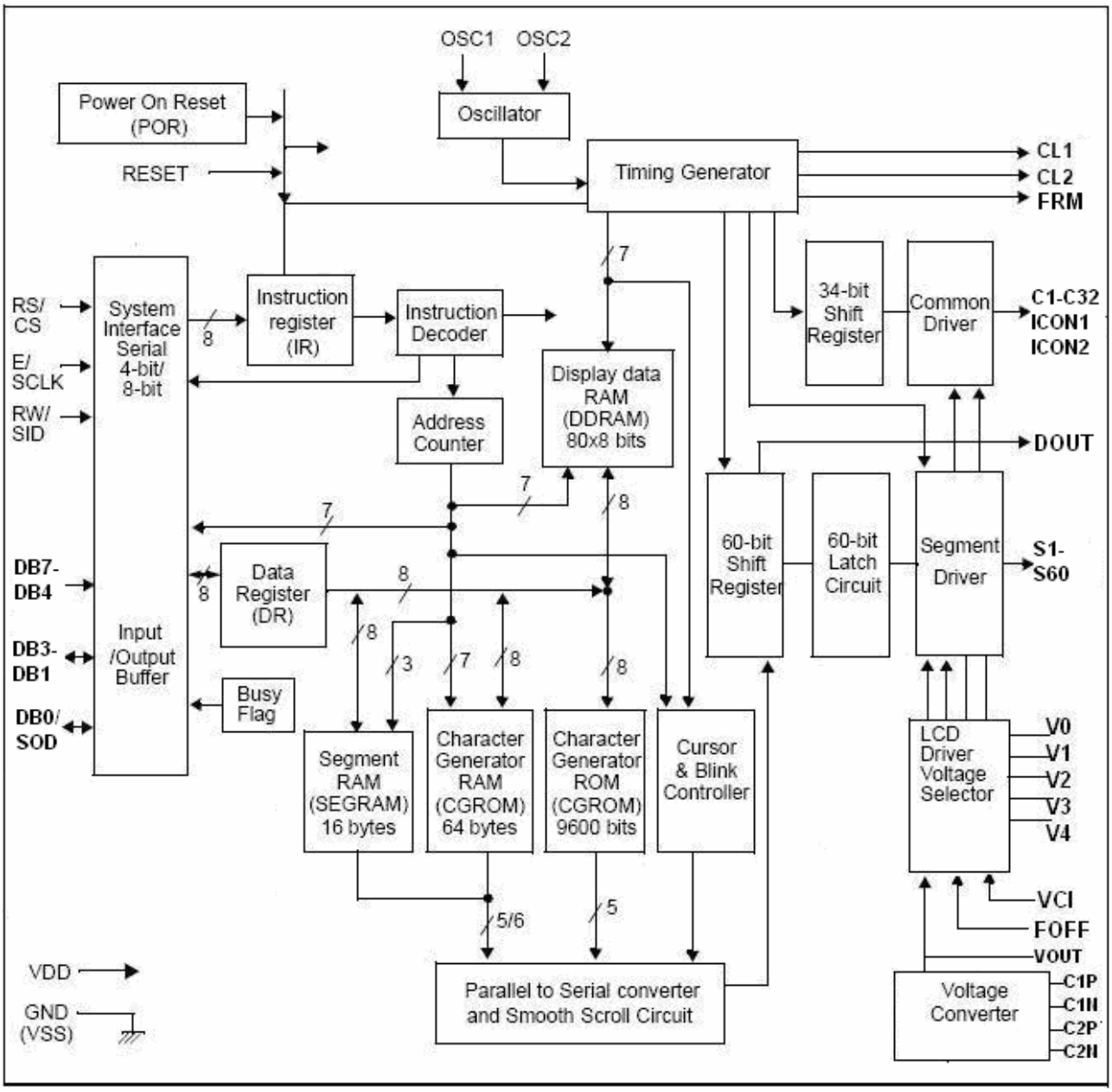
1) 5-dot font width

Display Line Numbers	Duty ratio	Single-chip operation		With Extension Driver	
		Displayable characters	Possible icons	Displayable characters	Possible icons
1	1/17	1 line of 24 characters	60	1 line of 52 characters	80
2	1/33	2 line of 24 characters	60	2 line of 32 characters	80
4	1/33	4 line of 12 characters	60	4 line of 20 characters	80

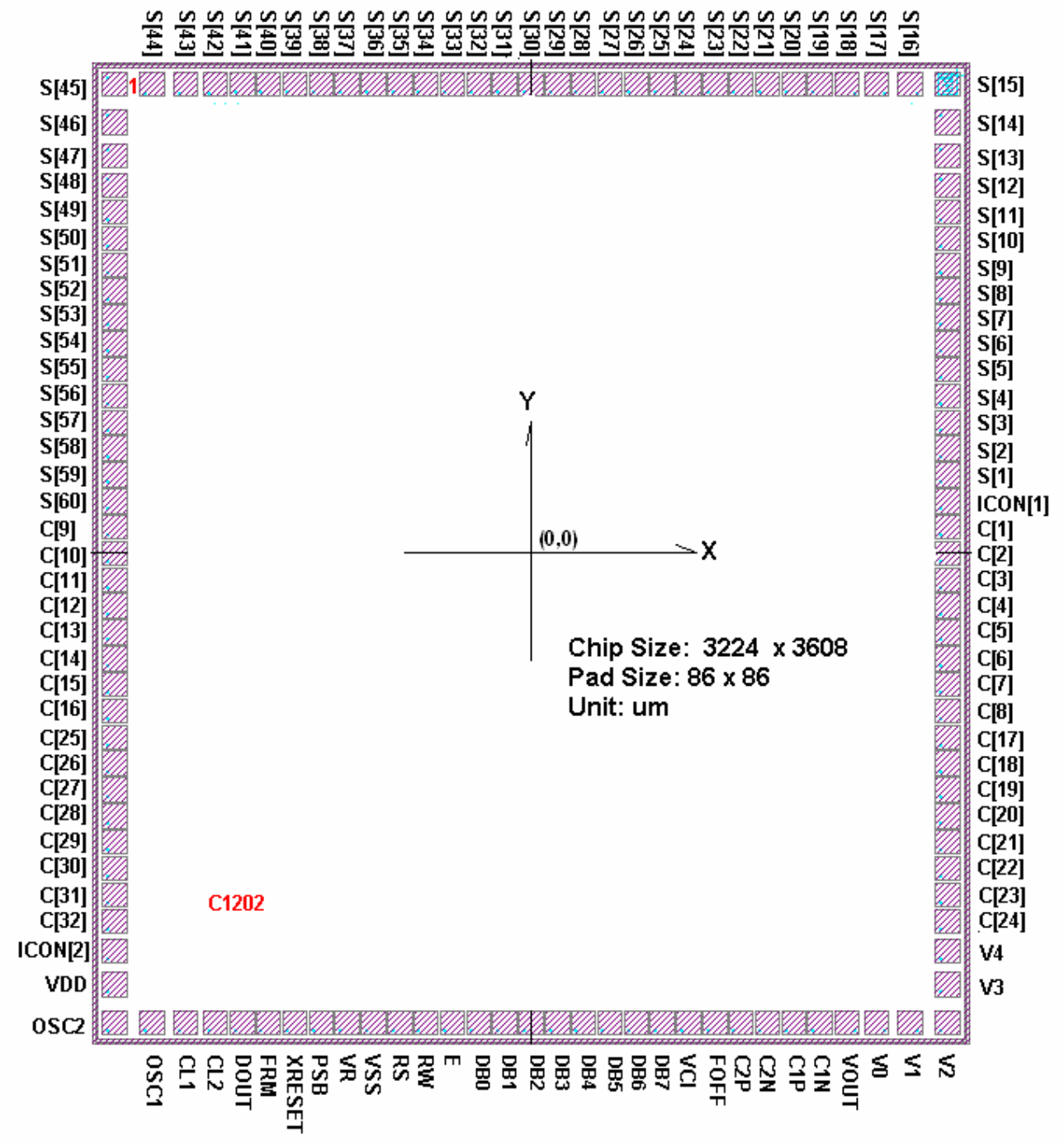
2) 6-dot font width

Display Line Numbers	Duty ratio	Single-chip operation		With Extension Driver	
		Displayable characters	Possible icons	Displayable characters	Possible icons
1	1/17	1 line of 20 characters	60	1 line of 50 characters	96
2	1/33	2 line of 20 characters	60	2 line of 30 characters	96
4	1/33	4 line of 10 characters	60	4 line of 20 characters	96

■ BLOCK DIAGRAM



■ PAD CONFIGURATION



■ PAD COORDINATE

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	S[45]	-1523	1715	33	ICON[2]	-1523	-1454
2	S[46]	-1523	1577	34	VDD	-1523	-1577
3	S[47]	-1523	1454	35	OSC2P	-1523	-1715
4	S[48]	-1523	1346	36	OSC1P	-1385	-1715
5	S[49]	-1523	1248	37	CL1	-1262	-1715
6	S[50]	-1523	1152	38	CL2	-1154	-1715
7	S[51]	-1523	1056	39	DOUT	-1056	-1715
8	S[52]	-1523	960	40	FRM	-960	-1715
9	S[53]	-1523	864	41	XRESET	-864	-1715
10	S[54]	-1523	768	42	PSB	-768	-1715
11	S[55]	-1523	672	43	VR	-672	-1715
12	S[56]	-1523	576	44	VSS	-576	-1715
13	S[57]	-1523	480	45	RS	-480	-1715
14	S[58]	-1523	384	46	RW	-384	-1715
15	S[59]	-1523	288	47	E	-288	-1715
16	S[60]	-1523	192	48	DB0	-192	-1715
17	C[9]	-1523	96	49	DB1	-96	-1715
18	C[10]	-1523	0	50	DB2	0	-1715
19	C[11]	-1523	-96	51	DB3	96	-1715
20	C[12]	-1523	-192	52	DB4	192	-1715
21	C[13]	-1523	-288	53	DB5	288	-1715
22	C[14]	-1523	-384	54	DB6	384	-1715
23	C[15]	-1523	-480	55	DB7	480	-1715
24	C[16]	-1523	-576	56	VCI	576	-1715
25	C[25]	-1523	-672	57	FOFF	672	-1715
26	C[26]	-1523	-768	58	C2P	768	-1715
27	C[27]	-1523	-864	59	C2N	864	-1715
28	C[28]	-1523	-960	60	C1P	960	-1715
29	C[29]	-1523	-1056	61	C1N	1056	-1715
30	C[30]	-1523	-1152	62	VOUT	1154	-1715
31	C[31]	-1523	-1248	63	V0	1262	-1715
32	C[32]	-1523	-1346	64	V1	1385	-1715

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
65	V2	1523	-1715	97	S[13]	1523	1454
66	V3	1523	-1577	98	S[14]	1523	1577
67	V4	1523	-1454	99	S[15]	1523	1715
68	C[24]	1523	-1346	100	S[16]	1385	1715
69	C[23]	1523	-1248	101	S[17]	1262	1715
70	C[22]	1523	-1152	102	S[18]	1154	1715
71	C[21]	1523	-1056	103	S[19]	1056	1715
72	C[20]	1523	-960	104	S[20]	960	1715
73	C[19]	1523	-864	105	S[21]	864	1715
74	C[18]	1523	-768	106	S[22]	768	1715
75	C[17]	1523	-672	107	S[23]	672	1715
76	C[8]	1523	-576	108	S[24]	576	1715
77	C[7]	1523	-480	109	S[25]	480	1715
78	C[6]	1523	-384	110	S[26]	384	1715
79	C[5]	1523	-288	111	S[27]	288	1715
80	C[4]	1523	-192	112	S[28]	192	1715
81	C[3]	1523	-96	113	S[29]	96	1715
82	C[2]	1523	0	114	S[30]	0	1715
83	C[1]	1523	96	115	S[31]	-96	1715
84	ICON[1]	1523	192	116	S[32]	-192	1715
85	S[1]	1523	288	117	S[33]	-288	1715
86	S[2]	1523	384	118	S[34]	-384	1715
87	S[3]	1523	480	119	S[35]	-480	1715
88	S[4]	1523	576	120	S[36]	-576	1715
89	S[5]	1523	672	121	S[37]	-672	1715
90	S[6]	1523	768	122	S[38]	-768	1715
91	S[7]	1523	864	123	S[39]	-864	1715
92	S[8]	1523	960	124	S[40]	-960	1715
93	S[9]	1523	1056	125	S[41]	-1056	1715
94	S[10]	1523	1152	126	S[42]	-1154	1715
95	S[11]	1523	1248	127	S[43]	-1262	1715
96	S[12]	1523	1346	128	S[44]	-1385	1715

■ PIN DESCRIPTION

Pin(No)	Input/ Output	Name	Description	Interface
VDD		Power Supply	For logical circuit(+3V,+5V)	Power Supply
VSS			0V (GND)	
V0~V4			Bias voltage level for LCD driving	
VCI	Input		Input voltage to the voltage regulator to Generate LCD drive voltage.	
S1~S60	Output	Segment Output	Segment signal output for LCD drive.	LCD
C1~C32 ICON1, ICON2	Output	Common Output	Common signal output for LCD drive.	LCD
OSC1, OSC2	Input (OSC1) Output (OSC2)	Oscillator	When using internal oscillator Rf resistor, If external clock is used, connect it to OSC1	External resistor/ Oscillator (OSC1)
CL1,CL2	Input	Latch(CL1)/Shift(CL2) Clock	Output latch clock and shift clock for extension driver	Extension driver
C1P,C1N C2P,C2N	Input	External capacitance input	To use the voltage converter (2 times/ 3 times), these pins must be connected to the external capacitance.	External capacitance
FRM	Output	Alternated signal for LCD driver output	The alternating signal to converter LCD driver waveform to AC for Extension driver.	Extension driver
DOUT	Output	Display data interface	Outputs extension driver data . (the 61th dot's data)	Extension driver
FOFF	Input	Internal Voltage Follower enable control	When FOFF="high", disable internal voltage follower When FOFF="Low", enable internal voltage follower	-
PSB	Input	Interface mode selection	When PSB="High": 8/4 bit bus mode. When PSB="Low": Serial mode.	-
XRESET	Input	Reset Pin	Initialized to Low	-

Pin(No)	Input/ Output	Name	Description	Interface
VOUT	Output	Converter output	Voltage converter output voltage	-
VR	Input	Reference input voltage	Reference voltage input to generate V0	-
RS/CS	Input	Register select/ Chip select	In bus mode, used as register selection input. When RS/CS="High", Data register is selected. When RS/CS="Low", instruction register is selected. In serial mode, used as chip selection input. When RS/CS="Low", selected. When RS/CS="High", not selected. (Low access enable)	MPU
RW/SID	Input	Read, Write/ Serial input data	In bus mode, used as read/ write selection input. When RW/SID="High", read operation. When RW/SID="Low", write operation. In serial mode used as serial clock input pin	MPU
E/SCLK	Input	Read, Write enable/ Serial clock	In bus mode, used as read/ write enable signal. In serial mode, used as serial clock input pin.	MPU
DB0/SOD	Input Output/ Output	Data bus 0 bit/ Serial output data	In 8-bit bus mode, used as low order bidirectional data bus. During 4-bit bus mode or serial mode, open these pins.	LCD
DB1~DB3	Input Output	Data bus 1~7	In 8-bit bus mode, used as low order bidirectional data bus. During 4-bit bus mode or serial mode, open these pin.	MPU
DB4~DB7			In 8-bit bus mode, used as high order bidirectional data bus. In 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output. During serial mode, open these pins.	

■ FUNCTION DESCRIPTION

◆ System Interface

This chip has all three kinds of interface type with MPU: serial, 4-bit and 8-bit bus.
Serial and bus (4-bit/8-bit) are selected by PSB input, and 4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. one is the data register (DR), the other is the instruction register(IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM/SEGRAM. Target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.
Hence, after MPU reads the DR data, the data in the next DDRAM/CGRAM/SEGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ SEGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use the RS/CS input pin in 4-bit/8-bit bus mode (PSB=“High”) or the RS bit in serial mode (PSB = “Low”).

Table 2. Various kinds of operations according to RS and R/W bits.

RS	R/W	Operatio
0	0	Instruction Write operation (MPU writes Instruction code into IR)
0	1	Read Busy flag (DB7) and address counter (DB0 ~ DB6)
1	0	Data Write operation (MPU writes data into DR)
1	1	Data Read operation (MPU reads data from DR)

◆ Busy Flag (BF)

When BF = “High”, it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = “Low” and R/W = “High” (Read Instruction Operation), through the DB7 port. Before executing the next instruction, be sure that BF is not high.

◆ Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80×8 bits (80 characters).

DDRAM address is set in the address counter (AC) as a hexadecimal number (Refer to Fig-1).

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

Fig-1 DDRAM Address

1) Display of 5-dot font width character

(1) 5-dot 1 line display

In the case of a 1-line display with 5-dot font, the address range of DDRAM is 00H ~ 4FH (Refer to Fig-2). When EXT= “High”, extension driver will be used.

Fig3 shows the example with 40 segment extension drivers added.

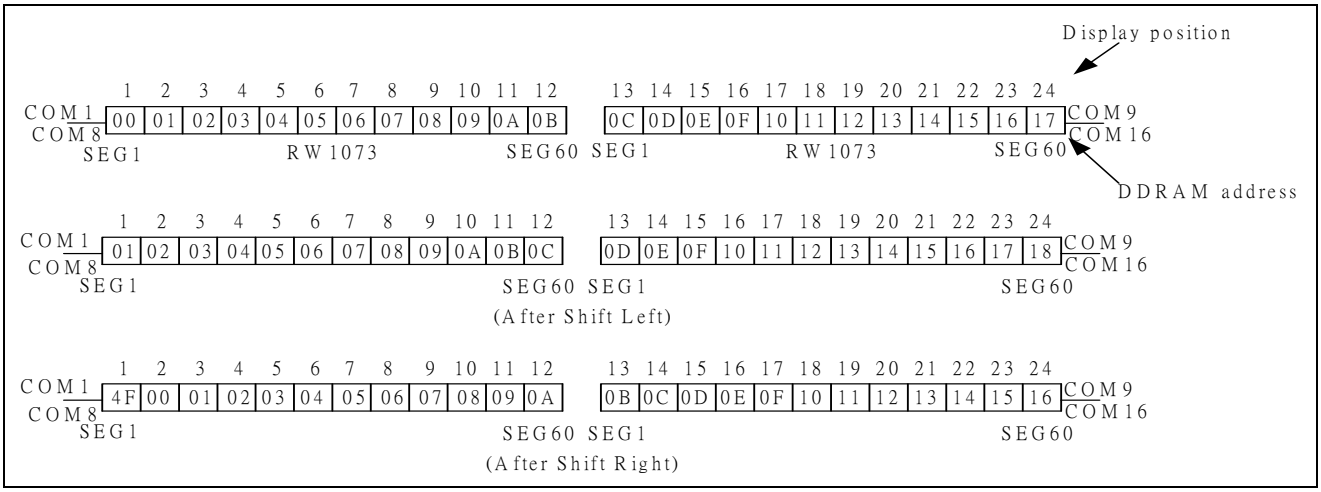


Fig-2. 1-line x 24 ch. display (5-dot font width)

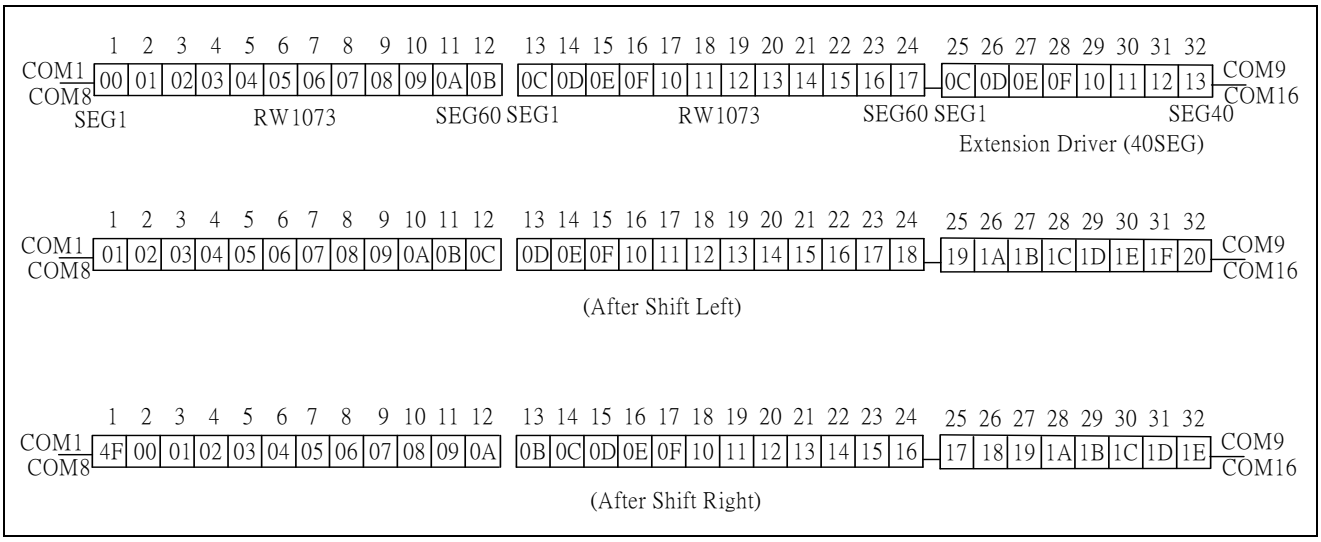


Fig-3. 1-line x 32 ch. display with 40 SEG. Extension driver (5-dot font width)

(2) 5-dot 2-line display

In the case of a 2-line display with 5-dot font, the address range of DDRAM is 00H–27H, and 40H–67H (Refer to Fig-4). When EXT = “High”, the extension driver will be used.

Fig-5 shows the example with 40 segment extension drivers added.

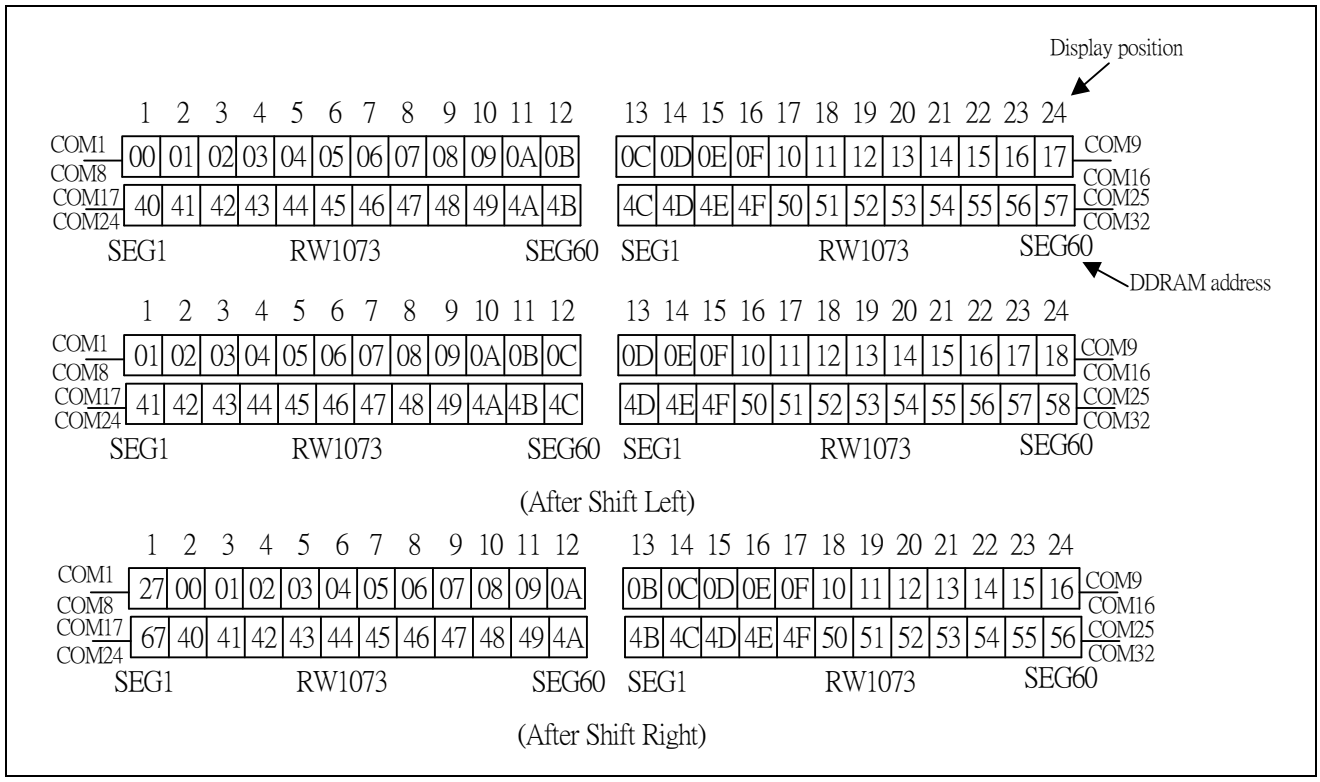


Fig-4. 2-line x 24 ch. display (5-dot font width)

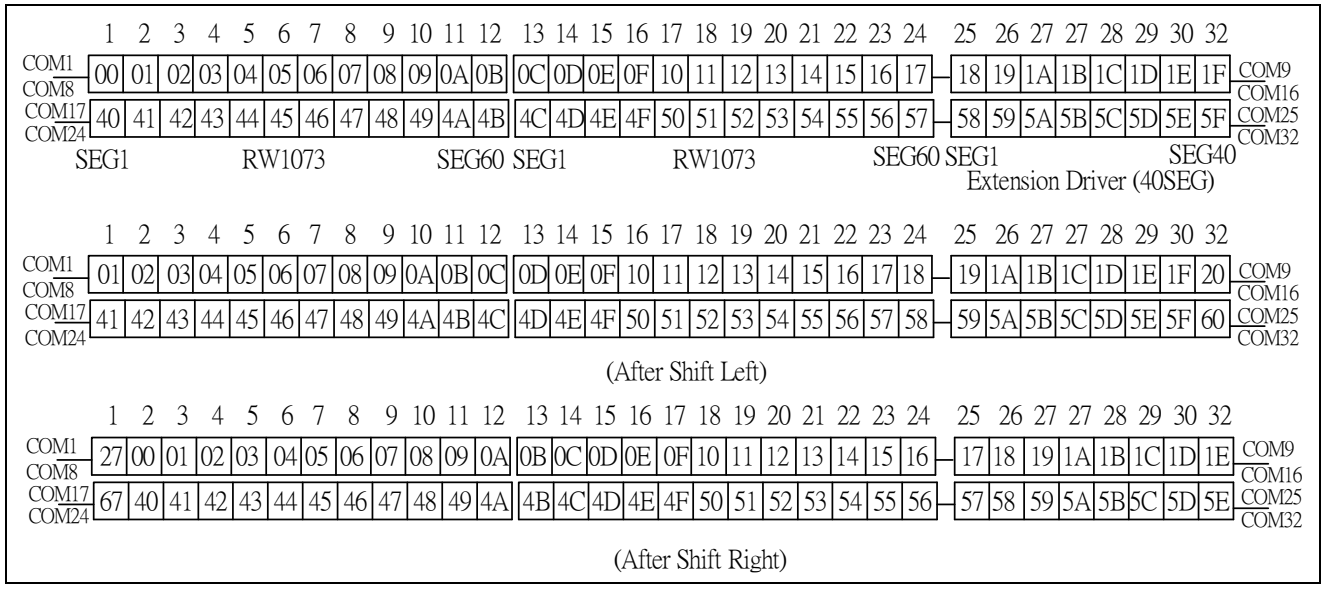


Fig-5. 2-line x 32 ch. display with 40 SEG. Extension driver (5-dot font width)

(3) 5-dot 4-line display

In the case of a 4-line display with 5-dot font, the address range of DDRAM is 00H–13H, 20H–33H, 40H–53H,60H–73H (Refer to Fig-6).

When EXT="High", extension driver will be used. Fig-7 shows the example with 40 segment extension drivers added.

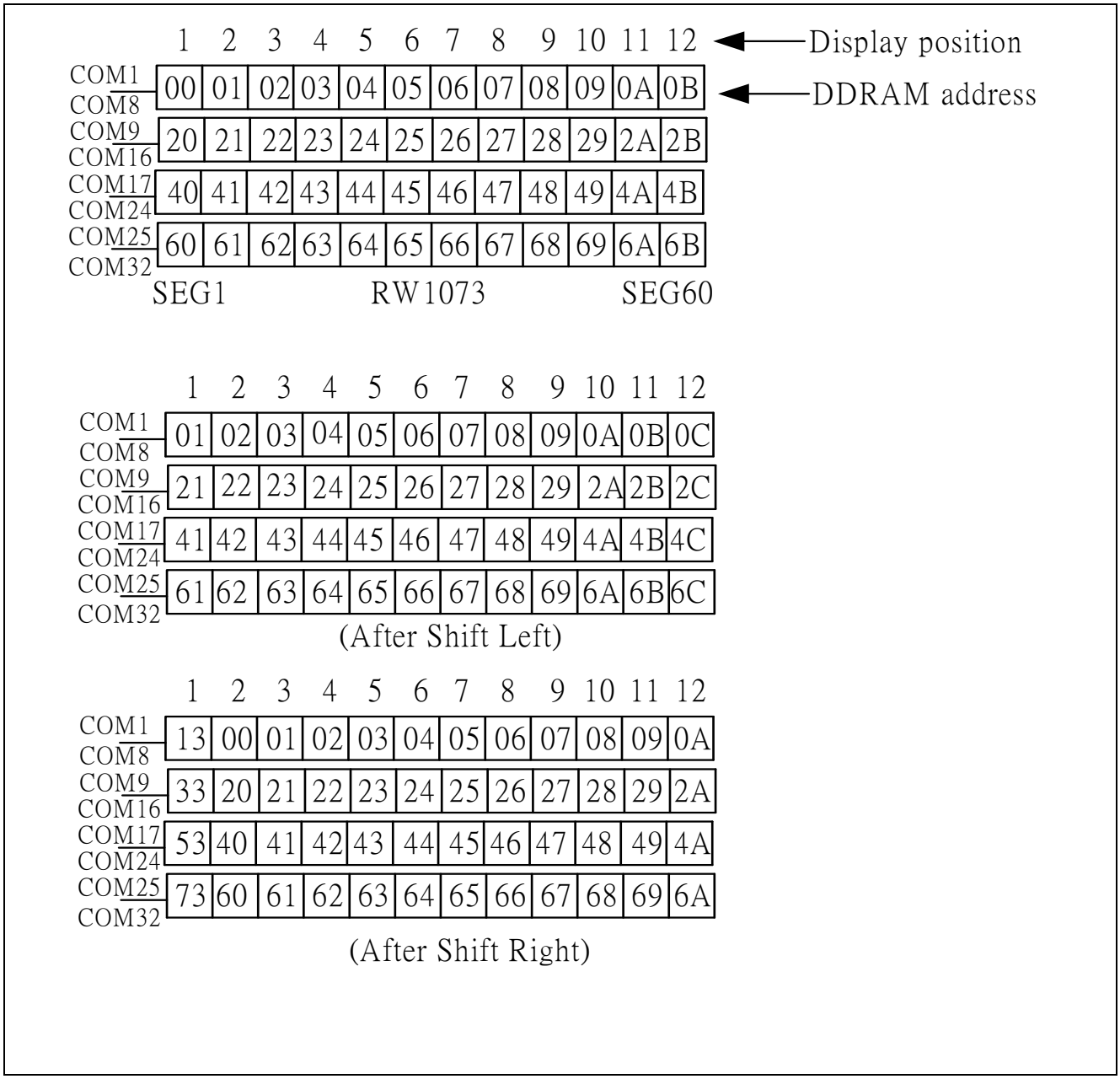


Fig-6. 4-line x 12 ch. display (5-dot font width)

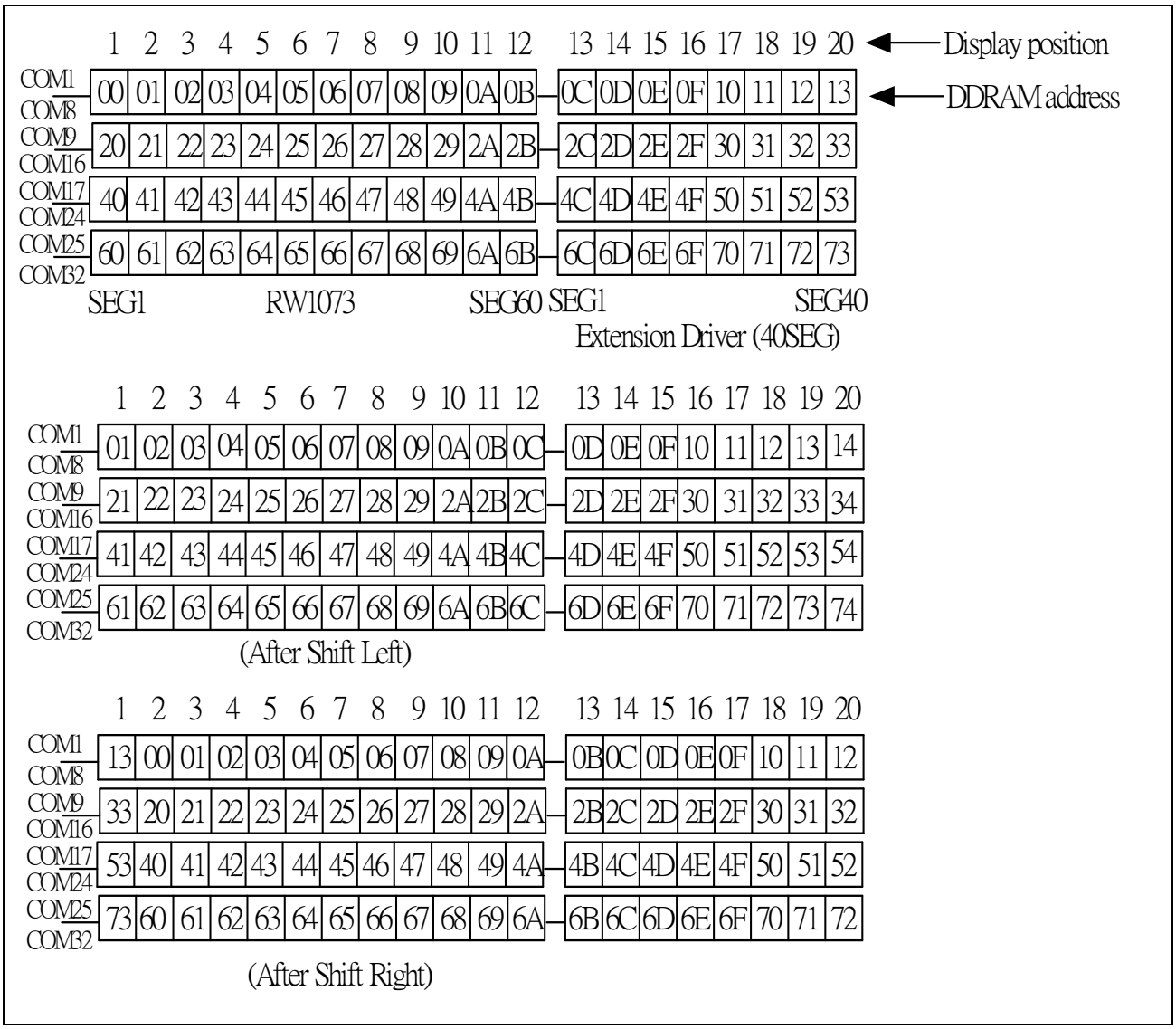


Fig-7. 4-line x 20 ch. display with 40 SEG. Extension driver (5-dot font width)

2) Display of 6-dot font width character

(1) 6-dot 1-line display

In the case of a 1-line display with 6-dot font, the address range of DDRAM is 00H–4FH

(Refer to Fig-8) When EXT = “High”, extension driver will be used.

Fig-9 shows the example with 40 segment extension driver added.

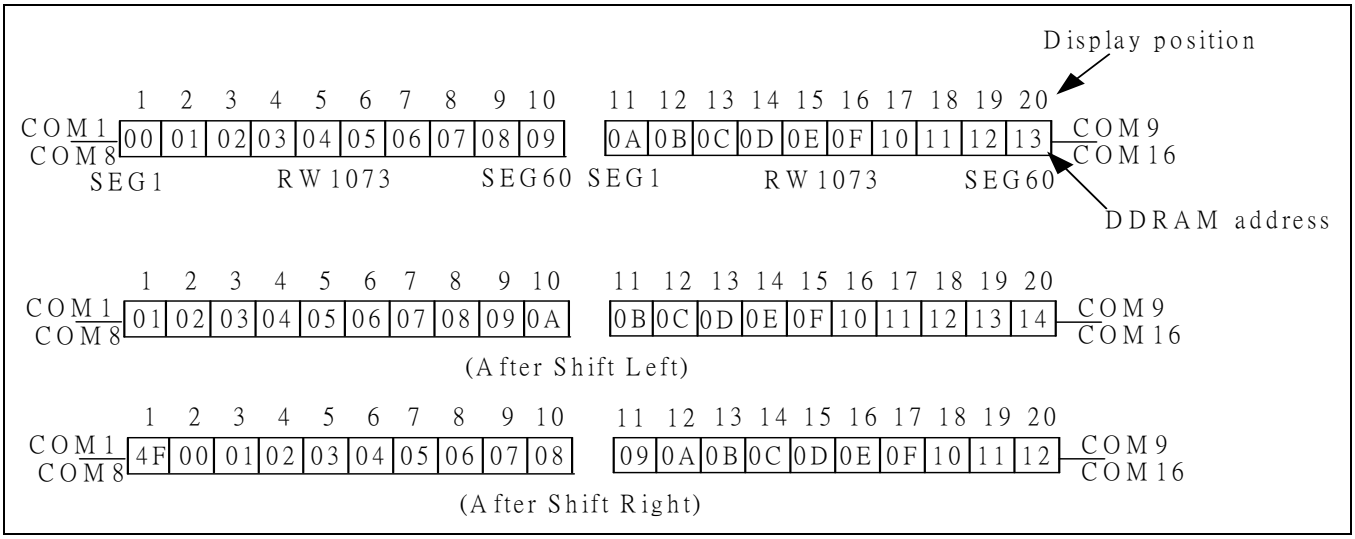


Fig-8. 1-line x 20 ch. display (6-dot font width)

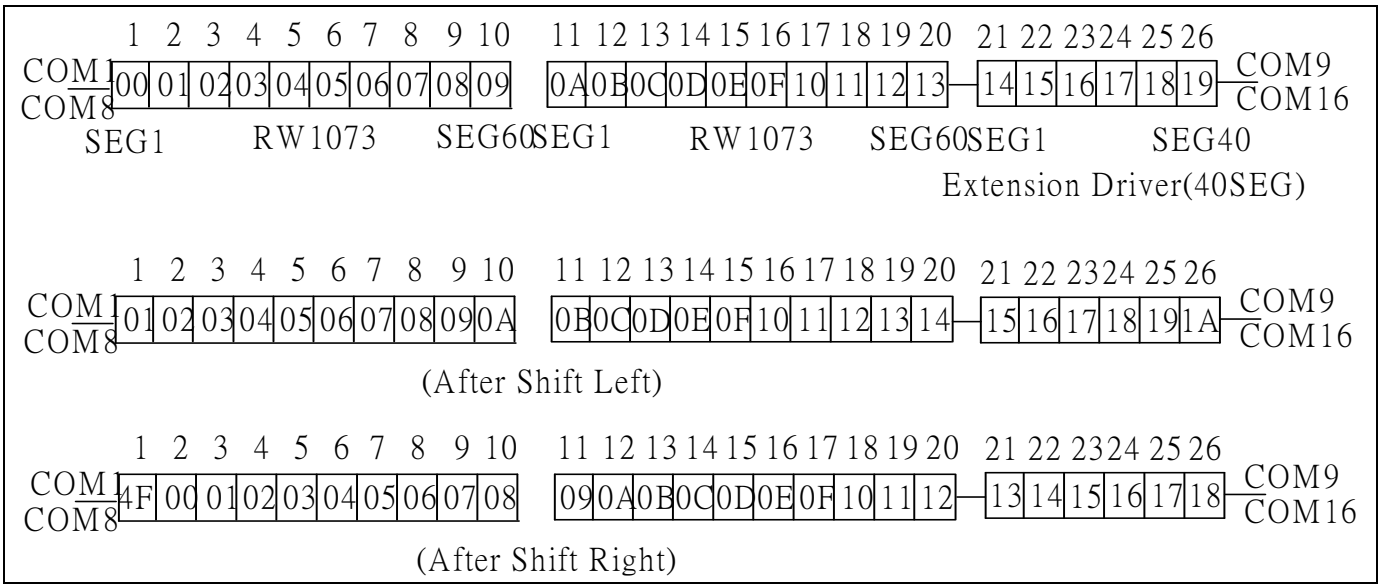


Fig-9. 1-line x 26 ch. display with 40 SEG. Extension driver (6-dot font width)

(2) 6-dot 2-line display

In the case of a 2-line display with 6-dot font, the address range of DDRAM is 00H–27H, and 40H–67H (Refer to Fig-10). When EXT = “High”, extension driver will be used.

Fig-11 shows an example with 40 segment extension drivers added.

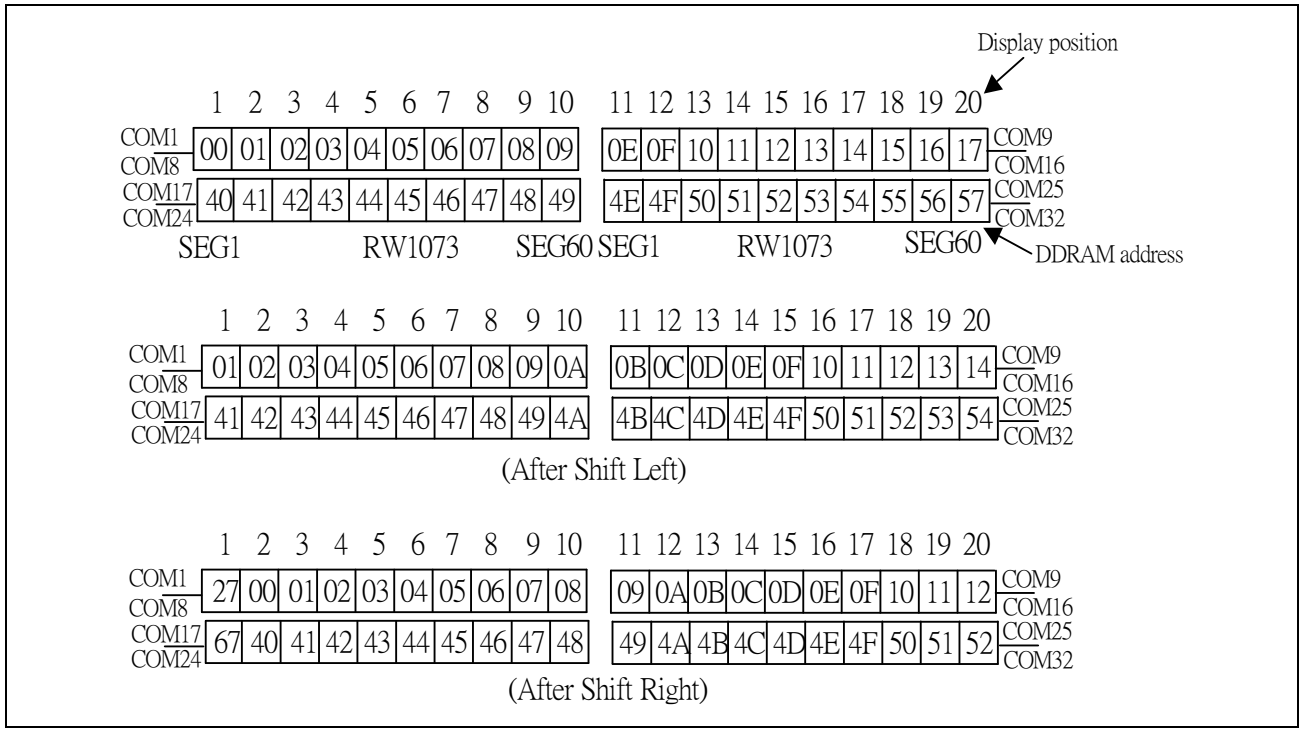


Fig-10. 2-line x 20 ch. display (6-dot font width)

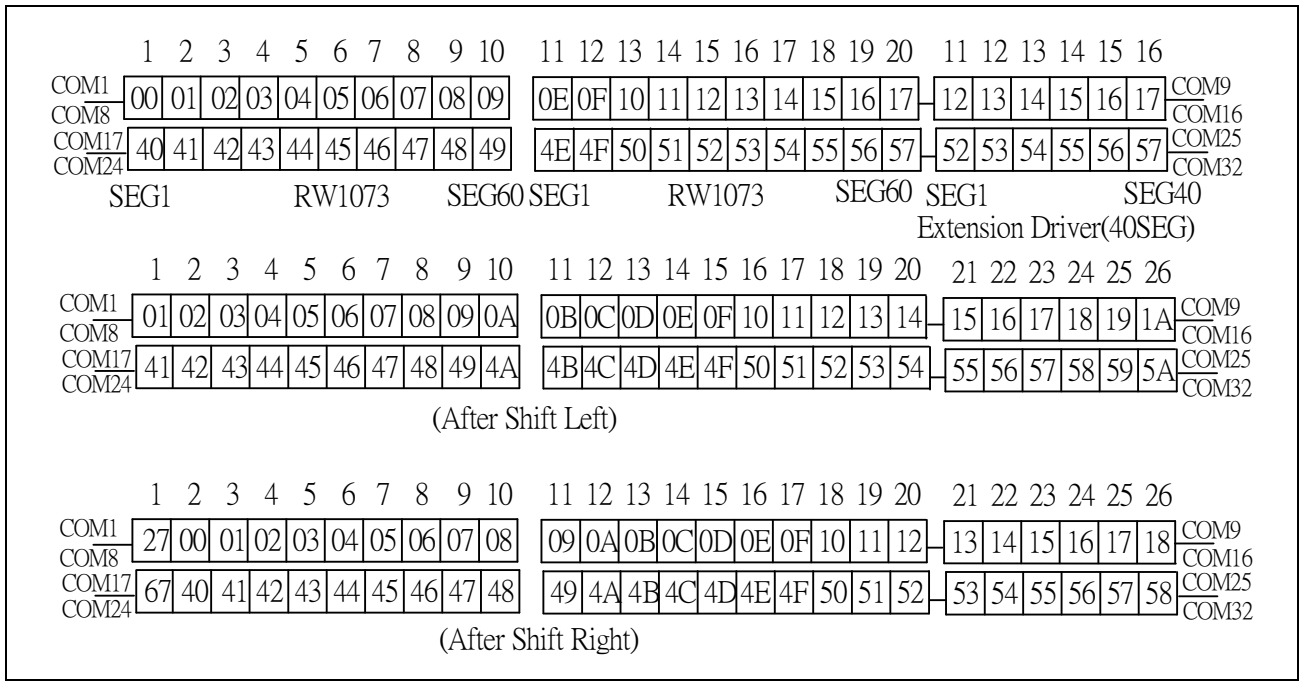


Fig-11. 2-line x 26 ch. display with 40 SEG. Extension driver (6-dot font width)

(3) 6-dot 4-line display

In the case of a 4-line display with 6-dot font, the address range of DDRAM is 00H–13H, 20H–33H, 40H–53H,60H–73H (Refer to Fig-12)

When EXT = “High”, the extension driver will be used.

Fig-13 shows the example with 40 segment extension drivers added.

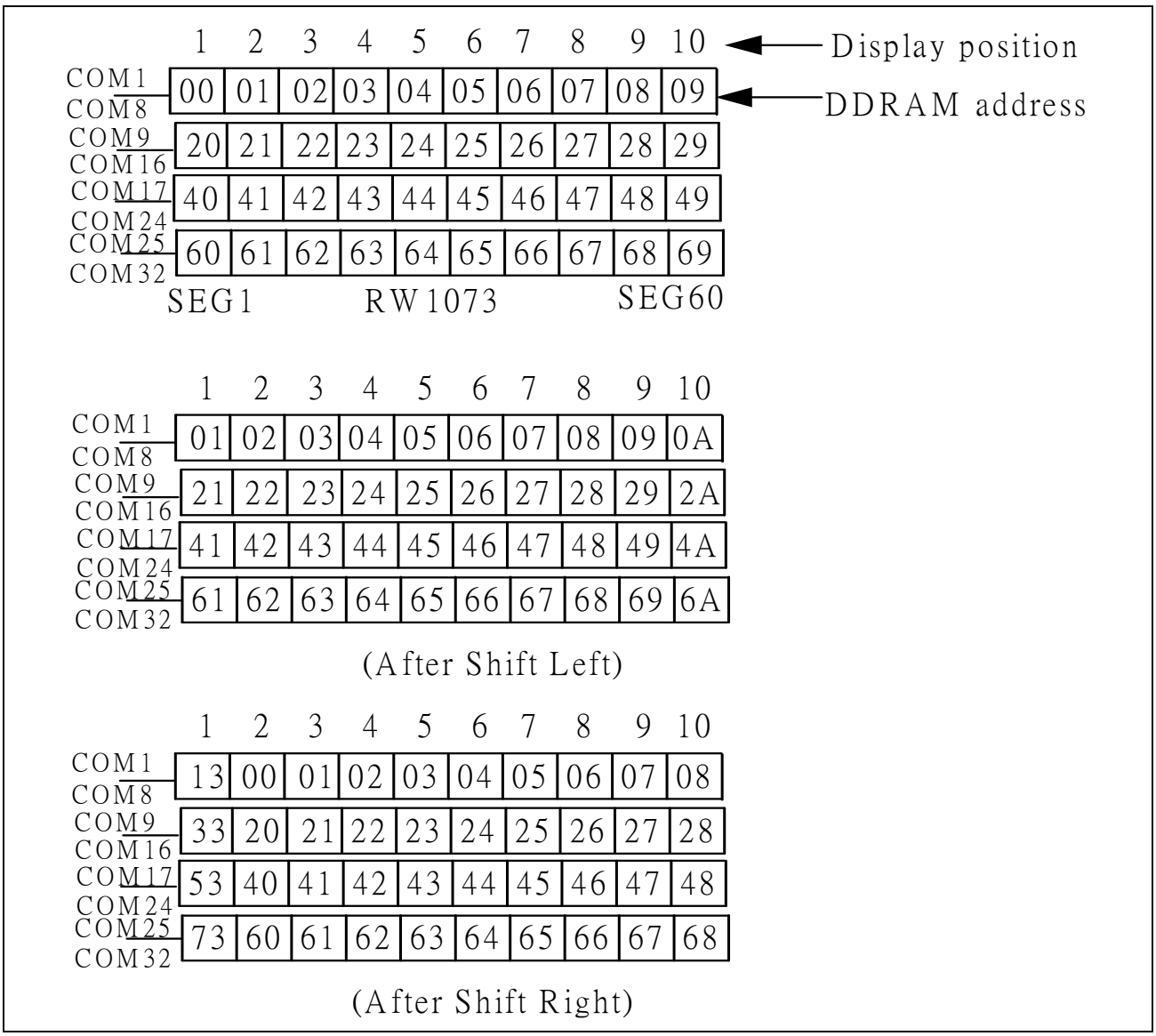


Fig-12. 4-line x 10 ch. display (6-dot font width)

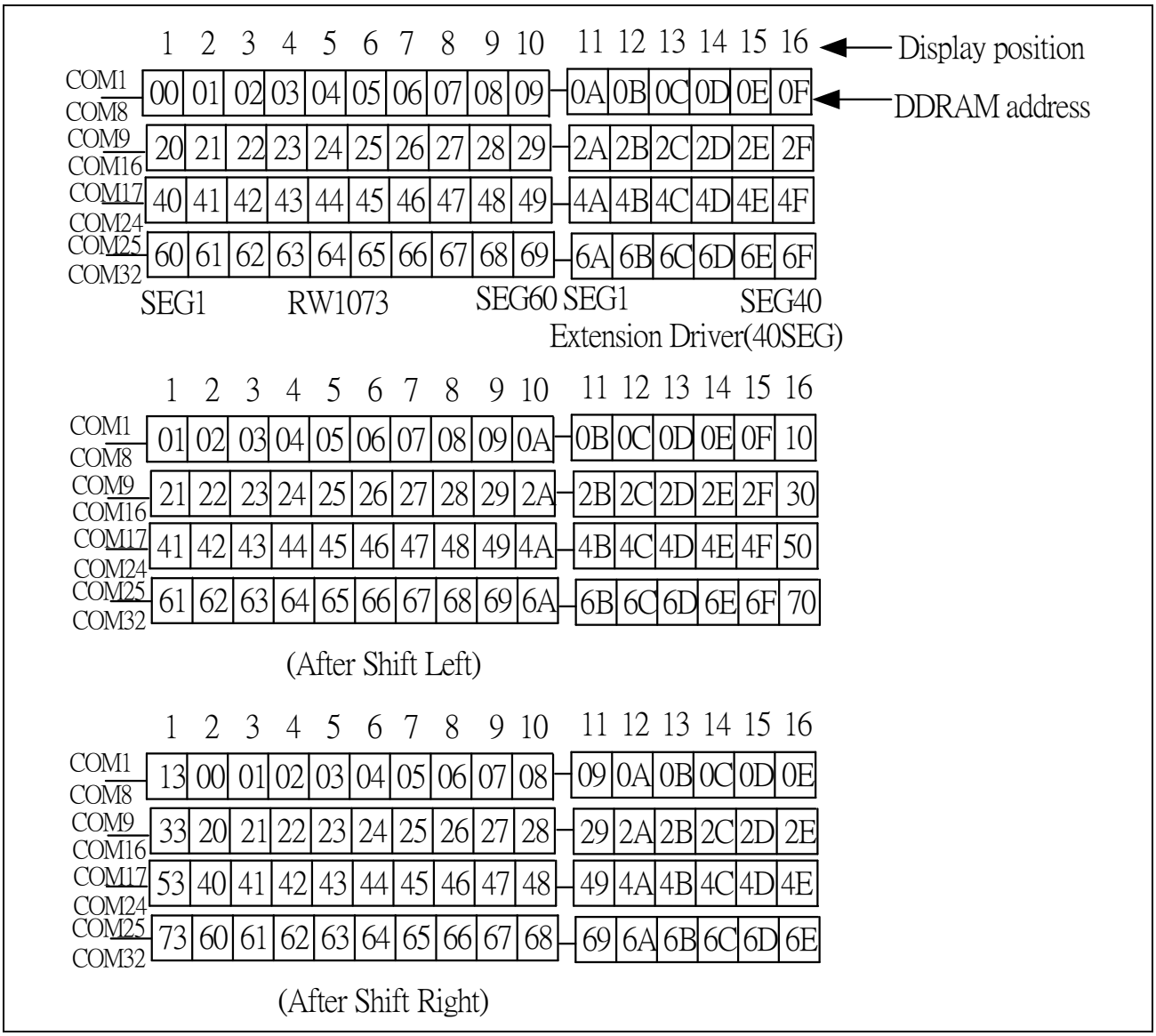


Fig-11. 2-line x 26 ch. display with 40 SEG. Extension driver (6-dot font width)

◆ **Timing Generation Circuit**

The timing generation circuit generates clock signals for internal operations.

◆ **Address Counter (AC)**

The address Counter (AC) stores DDRAM/CGRAM/SEGRAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1. When RS ="Low" and R/W = "High", AC can be read through DB0–DB6 ports.

◆ **Cursor/Blink Control Circuit**

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

◆ **LCD Driver Circuit**

The LCD Driver circuit has 34 common and 60 segment signals for LCD driving.

Data from SEGRAM/CGRAM/CGROM is transferred to a 60-bit segment latch serially, which is then stored to a 60-bit shift latch. When each common is selected by a 34-bit common register, segment data also outputs through a segment driver from a 100-bit segment latch.

In 1-line display mode, COM1 – COM16 have a 1/17 duty ratio, and in 2-line or 4-line mode, COM1 – COM32 have a 1/33 duty ratio.

■ CGRAM (Characters Generator RAM)

CGRAM has up to eight 5x8-dot characters. By writing data to CGRAM, user defined character can be use (Refer to Table 4)

1)5x8 dot Characters pattern

Character Code (DDRAM datat)								CGRAM address						CGRAM data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	B1	B0	X	0	(1)	(1)	(1)	0	Pattern 1
											0	0	1				(1)	0	0	0	(1)	
											0	1	0				(1)	0	0	0	(1)	
											0	1	1				(1)	(1)	(1)	(1)	0	
											1	0	0				(1)	0	(1)	0	0	
											1	0	1				(1)	0	0	(1)	0	
											1	1	0				(1)	0	0	0	(1)	
											1	1	1				0	0	0	0	0	
			⋮						⋮			⋮						⋮				⋮
0	0	0	0	X	1	1	1	1	1	1	0	0	0	B1	B0	X	(1)	0	0	0	(1)	Pattern 8
											0	0	1				(1)	0	0	0	(1)	
											0	1	0				(1)	0	0	0	(1)	
											0	1	1				(1)	1	(1)	1	(1)	
											1	0	0				(1)	0	(1)	0	(1)	
											1	0	1				(1)	0	(1)	0	(1)	
											1	1	0				0	(1)	0	(1)	0	
											1	1	1				0	0	0	0	0	

2)6x8 dot Characters pattern

Character Code (DDRAM datat)								CGRAM address						CGRAM data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	B1	B0	0	0	(1)	(1)	(1)	0	Pattern 1
											0	0	1			0	(1)	0	0	0	(1)	
											0	1	0			0	(1)	0	0	0	(1)	
											0	1	1			0	(1)	(1)	(1)	(1)	0	
											1	0	0			0	(1)	0	(1)	0	0	
											1	0	1			0	(1)	0	0	(1)	0	
											1	1	0			0	(1)	0	0	0	(1)	
											1	1	1			0	0	0	0	0	0	
			⋮						⋮			⋮						⋮				⋮
0	0	0	0	X	1	1	1	1	1	1	0	0	0	B1	B0	0	(1)	0	0	0	(1)	Pattern 8
											0	0	1			0	(1)	0	0	0	(1)	
											0	1	0			0	(1)	0	0	0	(1)	
											0	1	1			0	(1)	1	(1)	1	(1)	
											1	0	0			0	(1)	0	(1)	0	(1)	
											1	0	1			0	(1)	0	(1)	0	(1)	
											1	1	0			0	0	(1)	0	(1)	0	
											1	1	1			0	0	0	0	0	0	

NOTE: 1. When BE (Blink Enable bit) = “High”, blink is controlled by B1 and B0 bit.
In displaying 5-dot font width, when B1 = “1”, enabled dots in P0 – P4 ports will blink, and when B1 = “0” and B0 = “1”, enabled dots in P4 port will blink. When B1 = “0” and B0 = “0”, blinking will not occur.
In displaying 6-dot font width, when B1 = “1”, enabled dots of P0 – P5 ports will blink, and when B1 = “0” and B0 = “1”, enabled dots of P5 port will blink. When B1 = “0” and B0 = “0”, blinking will not occur.

2. “X”: Don’t care

■ SEGRAM (Segment Icon RAM)

SEGRAM has segment control data and segment pattern data. There are 2 ICON pins act as the COM line to display the icon SEGRAM data. The outputs of these 2 ICON pins are exactly the same. The higher 2-bits enable the data of SEGRAM to display icons. When used in 2/4-line display mode ICON1 & ICON2 do that.

The higher 2-bits are blinking control data, and the lower 6-bits are pattern data (Refer to Table 5 and Fig-14).

Table5. Relationship between SEGRAM addresses and display pattern

SEGRAM address				SEGRAM data display pattern															
				5-dot font width								6-dot font width							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	B1	B0	X	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	X	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	X	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	X	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	X	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	X	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	X	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	X	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	X	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	X	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	X	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	X	S56	S57	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	X	S61	S62	S63	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	X	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	X	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	X	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96

NOTE: 1. B1, B0: Blinking control bit

Control Bit			Blinking Port	
BE	B1	B0	5-dot font width	6-dot font width
0	X	X	No blink	No blink
1	0	0	No blink	No blink
1	0	1	D4	D5
1	1	X	D4 – D0	D5 – D0

2. S1 – S80: Icon pattern ON/OFF in 5-dot font width

   S1 – S96: Icon pattern ON/OFF in 6-dot font width

3. “X”: Don’t care

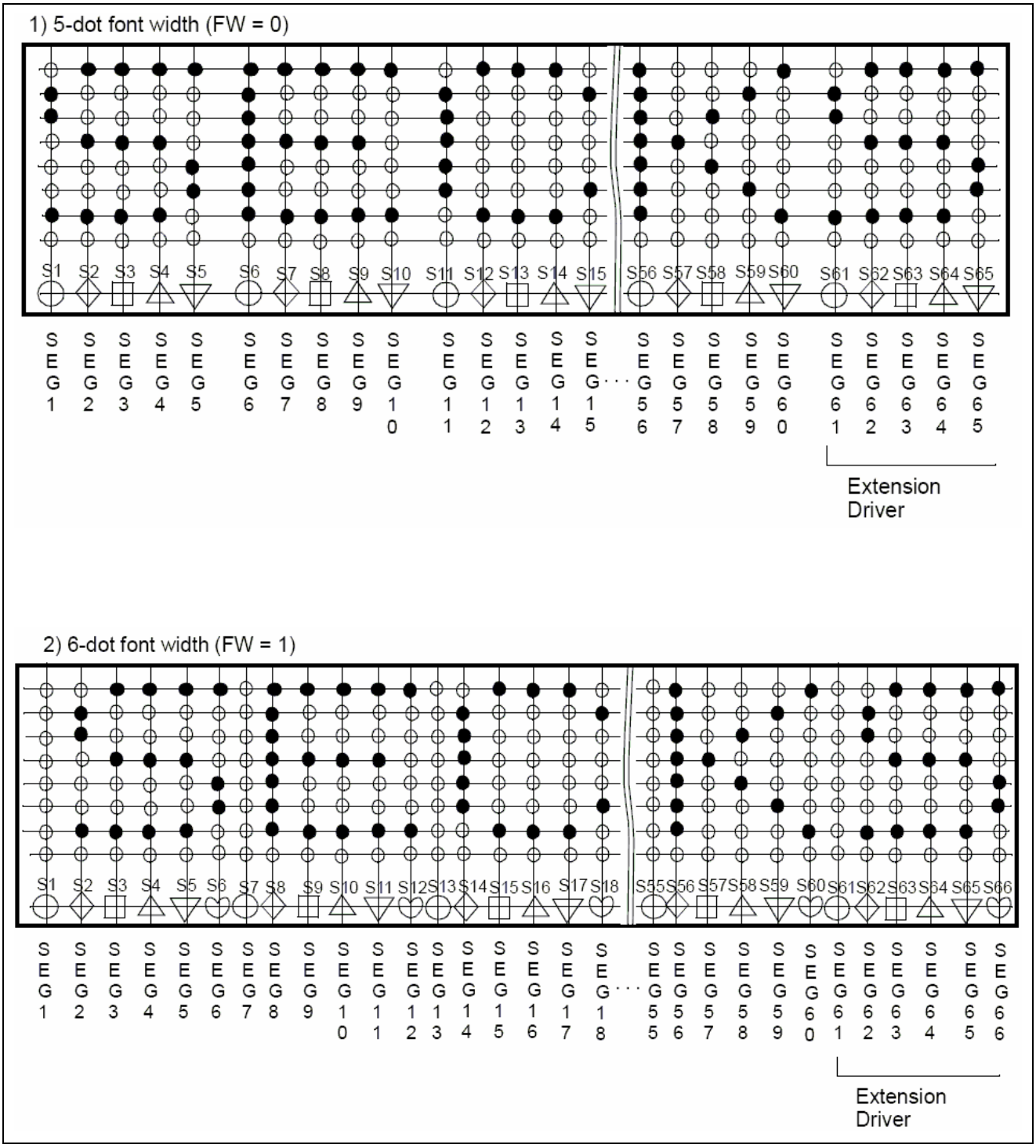


Fig-14. Relationship between SEGRAM and segment display

■ INSTRUCTION DESCRIPRION

◆ OUTLINE

To overcome the speed difference between the internal clock of RW1073 and the MPU clock, RW1073 performs internal operation by storing control information to IR or DR. The internal is determined according to the signal from the MPU, composed of read/write and data bus (Refer to Table 6 and Table 10). Instruction can be divided largely into four kinds.

(1) RW1073 function set instructions (set display methods .etc)
(2) Address set instruction to internal RAM.
(3) Data transfer instruction with internal RAM.
(4) Others.

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) reads high. Busy Flag check must precede the next instruction.

When an MPU program with Busy Flag (DB7) checking is made, 1/2 Fosc is necessary for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”.

■ INSTRUCTION DESCRIPTION

Table 6. Instruction Set

Instruction	RE	Instruction Code										Description	Execution Time(fosc =270KHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	**X**	**0**	**0**	0	0	0	0	0	0	0	1	Write “20H” to DDRAM. and set DDRAM address to “00H” from AC.	1.53ms
Return Home	**0**	**0**	**0**	0	0	0	0	0	0	1	X	Set DDRAM address “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Power Down Mode	**1**	**0**	**0**	0	0	0	0	0	0	1	PD	Set power down mode bit PD=”1”: power down mode set. PD=”0”: power down mode disable.	39uS
Entry Mode Set	**0**	**0**	**0**	0	0	0	0	0	1	I/D	S	Assign cursor moving direction, I/D=”1”: increment.. I/D=”0”: decrement. and display shift enable bit. S=”1”: make display shift of the enabled lines by the DS4-DS1 bits in the Shift Enable instruction. S=”0”: display shift disable.	39uS
	1	**0**	**0**	0	0	0	0	0	1	1	BID	Segment bidirectional function. BID=”1”: Seg60->Seg1. BID=”0”: Seg1->Seg60.	39uS
Display ON/OFF Control	**0**	**0**	**0**	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D=”1”: display on. D=”0”: display off. C=”1”: cursor on. C=”0”: cursor off. B=”1”: blink on. B=”0”: blink off.	39uS
Extended Function set	**1**	**0**	**0**	0	0	0	0	1	FW	B/W	NW	Assign font width; black/white inverting of cursor, and 4-line display mode bit. FW=”1”: 6-dot font width. FW=”0”: 5-dot font width B/W=”1”: black/white inverting of cursor enable. B/W=”0”: black/white inverting of cursor disable. NW=”1”: 4-line display mode. NW=”0”: 1-line or 2-line display mode.	39uS

Instruction	RE	Instruction Code										Description	Execution Time(fosc =270KHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Cursor or Display Shift	**0**	**0**	**0**	0	0	0	1	S/C	R/L	X	X	Cursor or display shift S/C="1": display shift. S/C="0": cursor shift R/L="1": shift to right. R/L="0": shift to left.	39uS
Shift Enable	**1**	**0**	**0**	0	0	0	1	DS4	DS3	DS2	DS1	(When DH="1") Determine the line for display shift. DS1="1/0": 1 st line display shift enable/disable. DS2="1/0": 2 nd line display shift enable/disable. DS3="1/0": 3 rd line display shift enable/disable. DS4="1/0": 1 th line display shift enable/disable.	39uS
Function Set	**0**	**0**	**0**	0	0	1	DL	N	RE (0)	DH	REV	Set interface data length, (DL="1": 8 bit, DL="0": 4bit), Number of display line when NW="0", (N="1": 2-line, N="0": 1-line), extension register, RE(0), shift enable, (DH="1": display enable, DH="0": display disable), and reverse bit (REV="1": reverse display,, REV="0": normal display)	39uS
	1	**0**	**0**	0	0	1	DL	N	RE (1)	BE	0	Set DL,N,RE("1") and CGRAM/SEGRAM blink enable (BE) (BE="1": CGRAM/SEGRAM blink enable, BE="0": CGRAM/SEGRAM blink disable)	39uS

Instruction	RE	Instruction Code										Description	Execution Time(fosc =270KHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set CGRAM Address	**0**	**0**	**0**	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39uS
Set SEGRAM Address	**1**	**0**	**0**	0	1	X	X	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter.	39uS
Set DDRAM Address	**0**	**0**	**0**	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39uS
Read Busy Flag and Address	**X**	**0**	**1**	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. (BF="1": busy state, BF="0": ready state)	0uS
Write Data	**X**	**1**	**0**	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ SEGRAM)	43uS
Read Data	**X**	**1**	**1**	D7	D6	D5	D4	D3	D2	D1	D0	Read data into internal RAM (DDRAM/CGRAM/ SEGRAM)	43uS

***NOTE:**

When an MPU program with Busy Flag (DB7) checking is made, 1/2 Fosc is necessary for executing the next instruction by the falling edge of the "E" signal after the Busy Flag (DB7) goes to "Low".

"X": Don't care.

◆ Display Clear

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, bringing the cursor to the left edge on first line of the display. Make entry mode increment (I/D = “1”).

◆ Return Home (RE=0)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is a cursor return home instruction.
Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

◆ Power Down Mode Set (RE=1)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	PD

Power down mode enable bit set instruction.
PD = “High”, it makes RW1073 suppress current consumption except the current needed for data storage by executing the next three functions.

1. Make the output value of all the COM/SEG ports VSS.
2. Make the COM/SEG output value of the extension driver VSS by setting D output to “High” and M output to “Low”.
3. Disable voltage converter to remove the current through the divide resistor of power supply. This instruction can be used as power sleep mode.

When PD = “Low”, power down mode becomes disabled.

◆ Entry Mode Set

RE=0:

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.
I/D: Increment / decrement of DDRAM address (cursor or blink)
When I/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM/SEGRAM operates the same as DDRAM, when reading from or writing to CGRAM/SEGRAM.

When S = “High”, after DDRAM write, the display of enabled line by DS1 - DS4 bits in the Shift Enable instruction is shifted to the right (I/D = “0”) or to the left (I/D = “1”). But it will seem as if the cursor does not move.
When S = “Low”, or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of display as the above function is not performed.

RE=1:

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	BID

Set the data shift direction of segment in the application set. BID: Data Shift Direction of Segment
When BID = “Low”, segment data shift direction is set to normal order, from SEG1 to SEG60.
When BID = “High”, segment data shift direction is set reversely, from SEG60 to SEG1.
By using this instruction, the efficiency of the application board area can be raised.
* The BID setting instruction is recommended to be set at the same time level as the function set instruction.
* DB0 bit must be set to “1”.

◆ Display ON/OFF Control (RE=0)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit.

When D = “High”, entire display is turned on.

When D = “Low”, display is turned off, but display data remains in DDRAM.

C: Cursor ON/OFF control bit

When C = “High”, cursor is turned on.

When C = “Low”, cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor Blink ON/OFF control bit

When B =“High”, cursor blink is on, that performs alternately between all the high data and display character at the cursor position. If fosc has a frequency of 270 kHz, blinking has a 370 ms interval.

When B =“Low”, blink is off.

◆ Extended Function Set (RE=1)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	F/W	B/W	NW

FW: Font Width control

When FW = “High”, display character font width is assigned to 6-dot, and the execution time becomes 6/5 times than that of the 5-dot font width.

The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0, including the left space bit of CGRAM (Refer to Fig-15).

When FW = “Low”, 5-dot font width is set.

B/W: Black/White Inversion enable bit

When B/W = “High”, black/white inversion at the cursor position is set. In this case, C/B bit of display ON/OFF control instruction becomes a “don’t care” condition. If fosc has frequency of 270 kHz, inversion has 370 ms intervals.

NW: 4 Line mode enable bit

When NW = “High”, 4-line display mode is set. In this case, N bit of function set instruction becomes a “don’t care” condition.

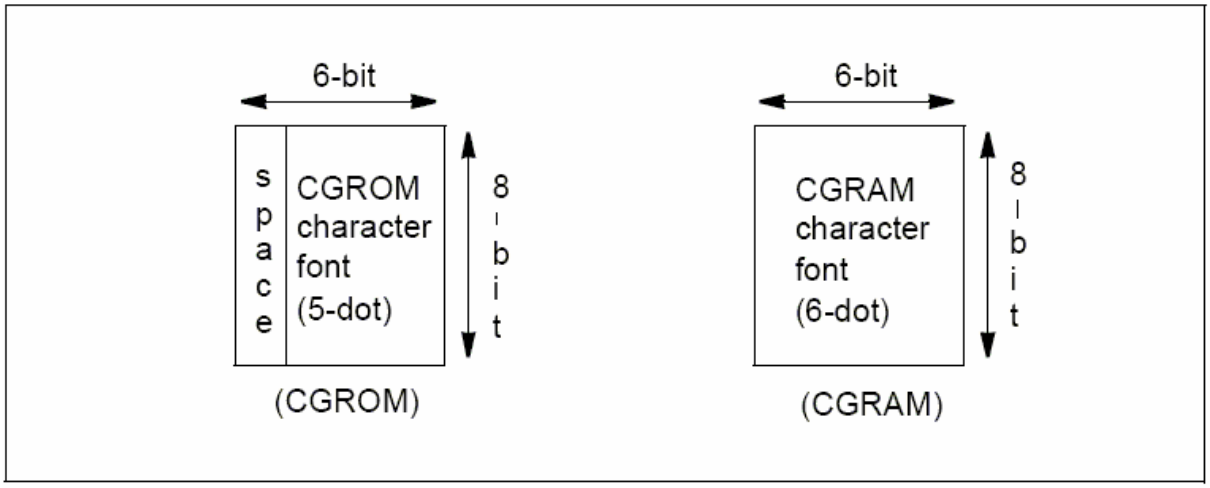


Fig-15. 6-dot font width CGROM/CGRAM

◆ Cursor or Display Shift (RE=0)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifts right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data (Refer to Table 7).
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. In 4-line mode, cursor moves to the next line, only after every 20th digit of the current line.
Note that display shift is performed simultaneously in all the lines enabled by DS1-DS4 in the Shift Enable instruction.
When displayed data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed. During low power consumption mode, display shift may not be performed normally.

Table 7. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, ADDRESS COUNTER is decreased by 1
0	1	Shift cursor to the right, ADDRESS COUNTER is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

◆ Shift Enable (RE=1)

DH=1

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	DS4	DS3	DS2	DS1

DS: Display Shift per Line Enable

This instruction selects the line to be shifted according to each line mode in display shift right/left instruction. DS1, DS2, DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line.

If DS1 and DS2 are set to “High” (enable) in 2-line mode, only 1st line is shifted, and the 2nd line is not shifted. When only DS1=“High”, only half of the 1st line is shifted. If all the DS bits (DS1 to DS4) are set to “Low” (disable), no display is shifted.

Table 8. Relationship between DS and COM signal

Enable bit	Enable common signals during shift	Description
DS1	COM1~COM8	The part of display line that corresponds to enable common signal can be shifted.
DS2	COM9~COM16	
DS3	COM17~COM24	
DS4	COM25~COM32	

◆ Function Set

RE=0

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE(0)	DH	REV

DL: Interface data length control bit

When DL = “High”, it means 8-bit bus mode with MPU.

When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode. In 4-bit bus mode, it is required to transfer 4-bit data twice.

N: Display line number control bit

It is variable only when NW bit of extended function set instruction is Low.

When N = “Low”, 1-line display mode is set.

When N = “High”, 2-line display mode is set.

When NW = “High”, N bit is invalid, 4-line mode independent of N bit.

RE: Extended function registers enable bit

At this instruction, RE must be “Low”.

DH: Display shift enable selection bit.

When DH = “High”, enables display shift per line.

When DH = “Low”, enables smooth dot scroll.

REV: Reverse enable bit

When REV = “High”, all the display data are reversed. i.e., all the white dots become black and black dots become white.

When REV = “Low”, the display mode is set to normal display.

RE=1

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE(1)	BE	0

DL: Interface data length control bit

When DL = “High”, it means 8-bit bus mode with MPU.

When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it is required to transfer 4-bit data twice.

N: Display line number control bit

It is variable only when NW bit of extended function set instruction is Low.

When N = “Low”, 1-line display mode is set.

When N = “High”, 2-line display mode is set.

When NW = “High”, N bit is invalid, 4-line mode independent of N bit.

RE: Extended function registers enable bit

When RE =“High”, extended function set registers, SEGRAM address set registers, BID bit, DS bits of shift enable instruction and BE bits of function set register can be accessed.

BE: CGRAM/SEGRAM data blink enable bit

BE = “High”, makes user font of CGRAM and segment of SEGRAM blinking.

The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

◆ Set CGRAM Address (RE=0)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

◆ Set SEGRAM Address (RE=1)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	X	X	AC3	AC2	AC1	AC0

Set SEGRAM address to AC.
This instruction makes SEGRAM data available from MPU.

◆ Set DDRAM Address (RE=0)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
In 1-line display mode (N = 0, NW = 0), DDRAM address is from “00H” to “4FH”.
In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from “00H” to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.
In 4-line display mode (NW = 1), DDRAM address is from “00H” to “13H” in the 1st line, from“20H” to “33H” in the 2nd line, from “40H” to “53H” in the 3rd line and from “60H” to “73H” in the 4th line.

◆ Read Busy Flag and Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether RW1073 is in internal operation or not. If the resultant BF is High, The internal operation is in progress and should wait until BF to be Low, which by then the next instruction can be performed. In this instruction the value of address counter can also be read.

◆ Write Data to RAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.
The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, SEGRAM address set.
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

◆ Read Data from RAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that is read first is invalid, as the direction of AC is not determined. If RAM data is read several times without RAM address set instructions before read operation, the correct RAM data can be obtained from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfers RAM data to output data register.
After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM/SEGRAM read operation, display shift may not be executed correctly.
* In the case of RAM write operation, AC is increased/decreased by 1 as in read operation after this. In this time, AC indicates the next address position, but the previous data can only be read by read instruction.

■ INTERFACE WITH MPU

RW1073 can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU. Hence, both types, 4 or 8-bit MPU can be used. In case of 4-bit bus mode, data transfer is performed by twice to transfer 1 byte data.

(1) When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first, higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by twice. Busy Flag outputs “High” after the second transfer is ended.

(2) When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.

(3) If PSB port is set to “Low”, serial transfer mode is set.

■ Interface with MPU in Bus Mode

◆ Interface with 8-bit MPU

If 8-bit MPU is used, RW1073 can connect directly with that. In this case, port E, RS, R/W and DB0 to DB7 need to interface each other. Example of timing sequence is shown below.

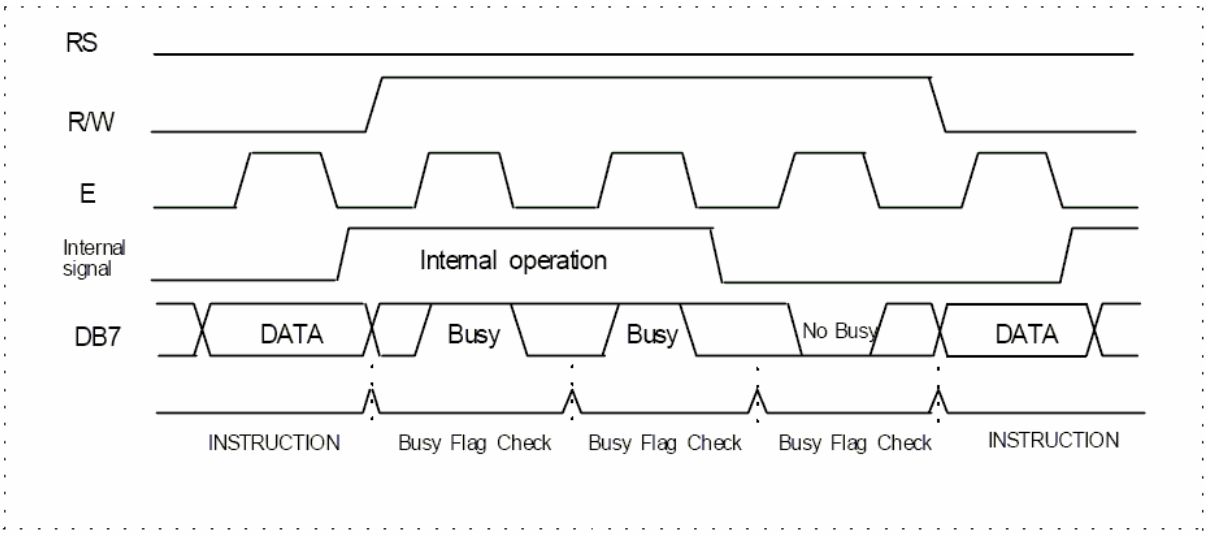


Fig-17. Example of 8-bit Bus Mode Timing Sequence

◆ Interface with 4-bit MPU

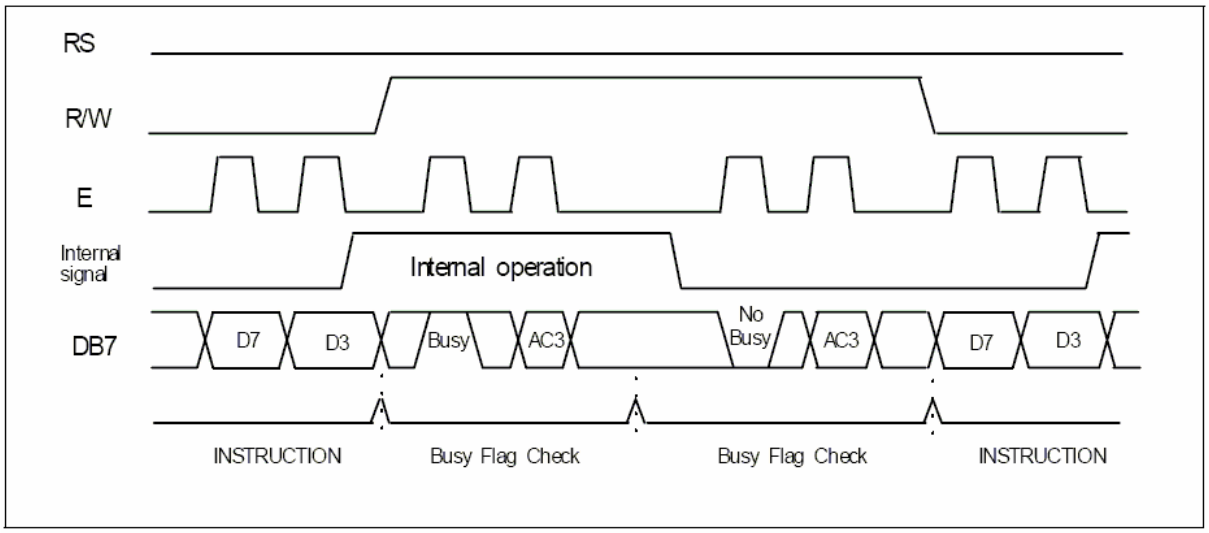


Fig-18. Example of 4-bit Bus Mode Timing Sequence

■ Interface with MPU in Serial Mode

When PSB pin input is “Low”, serial interface mode is started. At this time, all three ports, SCLK (synchronizing transfer clock), SID (serial input data), and SOD (serial output data), are used. If RW1073 is to be used with other chips, chip select port (CS) can be used. By setting CS to “Low”, RW1073 can receive SCLK input. If CS is set to “High”, RW1073 resets the internal transfer counter.

Before transferring real data, start byte has to be transferred. It is composed of succeeding 5 “High” bits, read write control bit (R/W), register selection bit (RS), and end bit that indicates the end of start byte. Whenever succeeding 5 “High” bits are detected by RW1073, it resets the serial transfer counter and prepares to receive next in formations.
The next input data is the register selection bit which determines which register is to be used, and read write control bit that determines the direction of data. Then end bit is transferred, which must have “Low” value t show the end of start byte. (Refer to Fig 19, Fig 20)

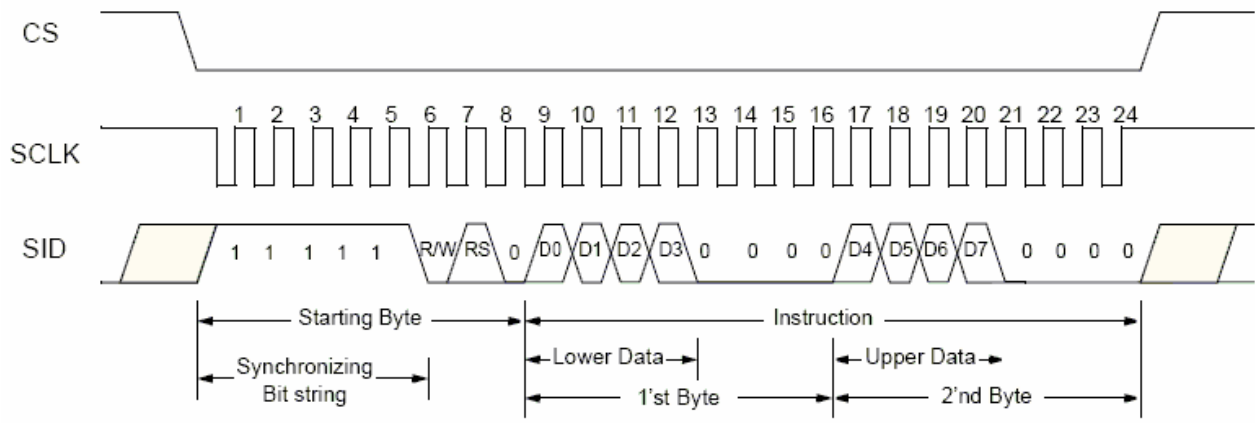
◆ Write Operation (R/W = 0)

After start byte is transferred from MPU to RW1073, 8-bit data is transferred which is divided into 2 bytes, each byte has 4 bit's real data and 4 bit's partition token data. For example, if real data is "10110001" (D0 - D7), then serially transferred data becomes "1011 0000 0001 0000" where 2nd and 4th 4 bits must be "0000" for safe transfer.
To transfer several bytes continuously without changing R/W bit and RS bit, start byte transfer is needed only at first starting time.
i.e., after the first start byte is transferred, real data succeeding can be transferred.

◆ Read Operation (R/W = 1)

After start byte is transferred to RW1073, MPU can receive 8-bit data through the SOD port at a time from the LSB. Waiting time is needed to insert between start byte and data reading, as internal reading from RAM requires some delay. Continuous data reading is possible such as serial write operation. It also needs only one start bytes, only if some delay between reading operations of each byte is inserted. During the reading operation, RW1073 observes succeeding 5 "High" from MPU. If detected, RW1073 restarts serial operation at once and prepares to receive RS bit. So in continuous reading operation, SID port must be "Low".

◆ Serial Write operation



◆ Serial Read operation

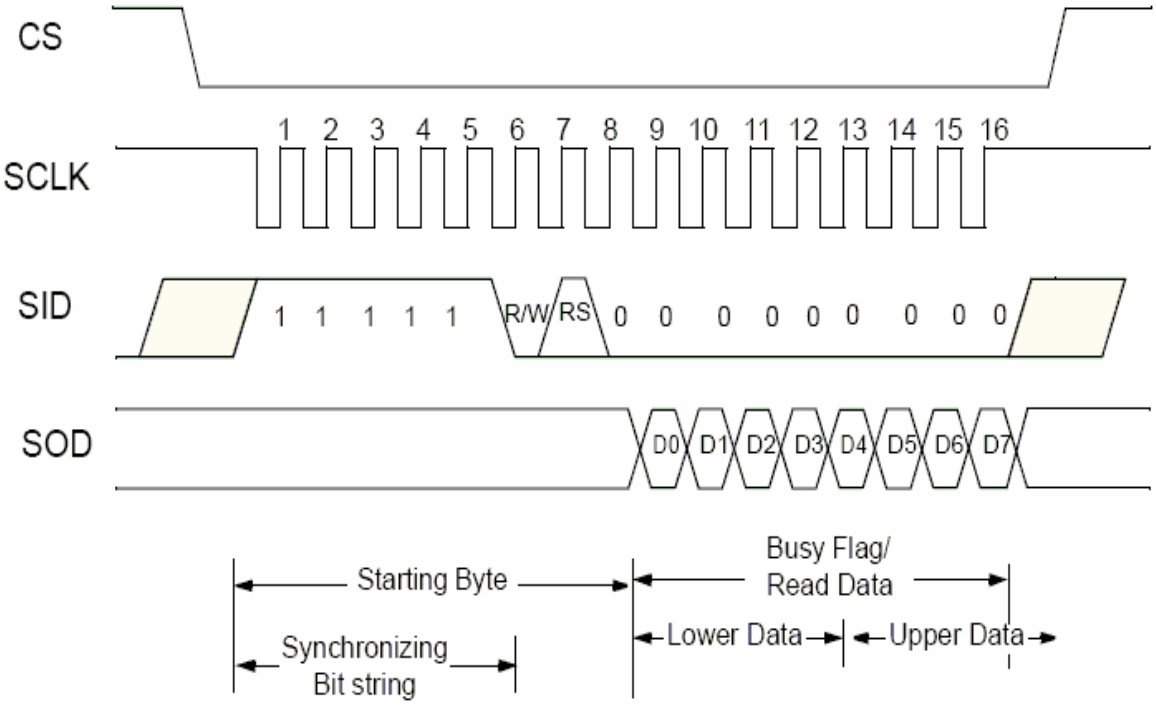
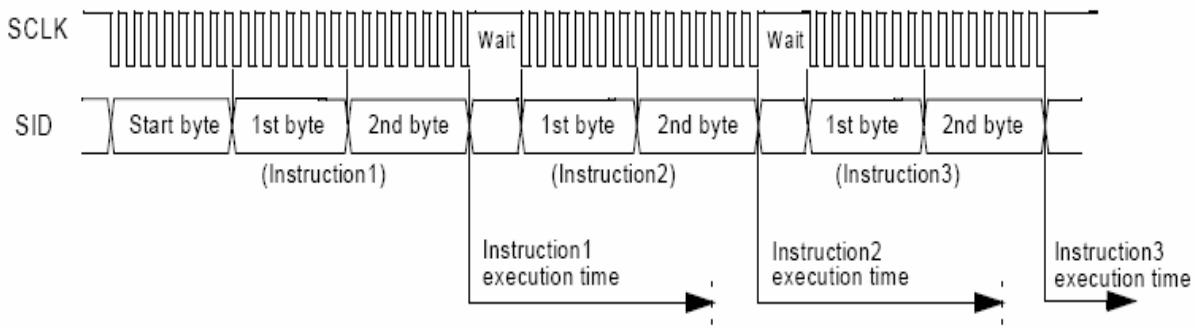


Fig-19. Timing Diagram of Serial Data Transfer

(1) Continuous Write Operation



(2) Continuous Read Operation

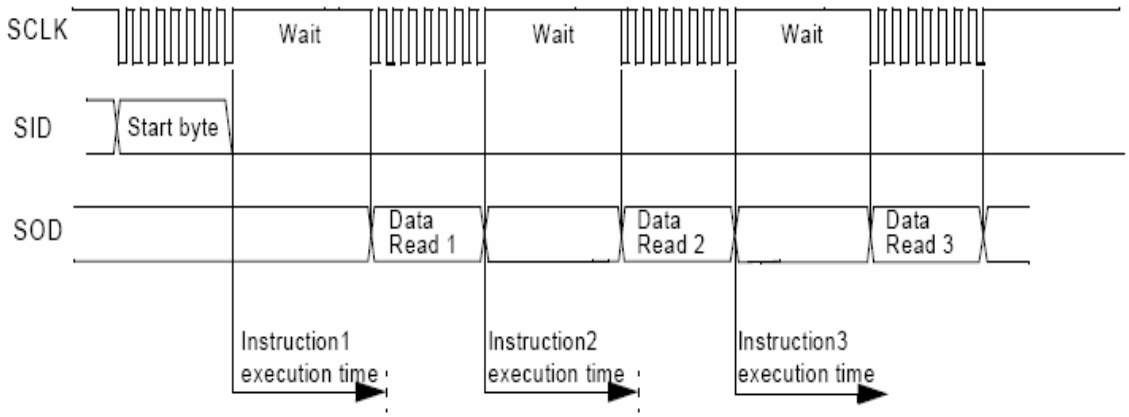
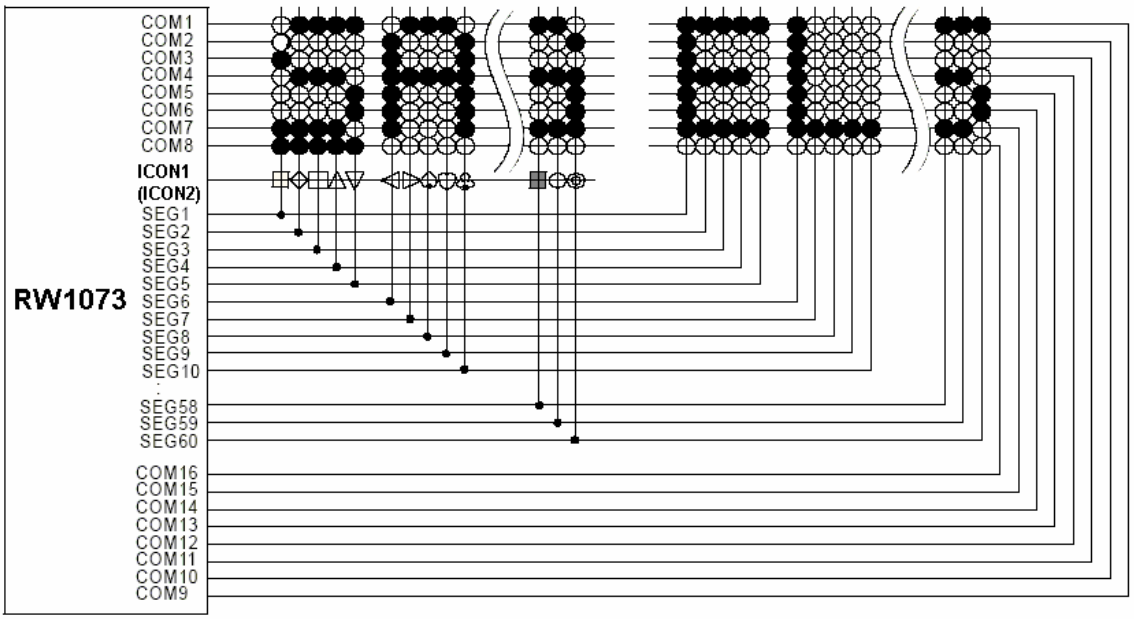


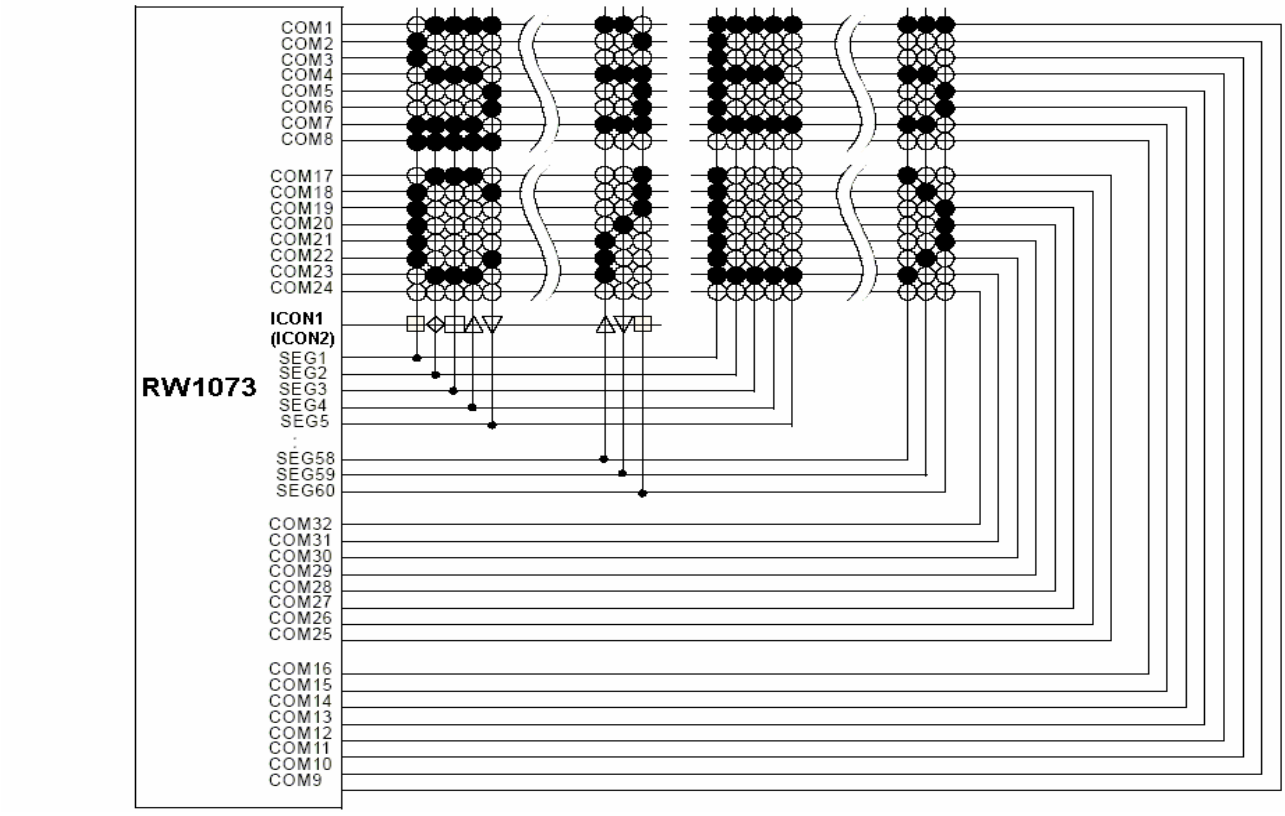
Fig-20. Timing Diagram of Continuous Data Transfer

■ APPLICATION INFORMATION ACCORDING TO LCD

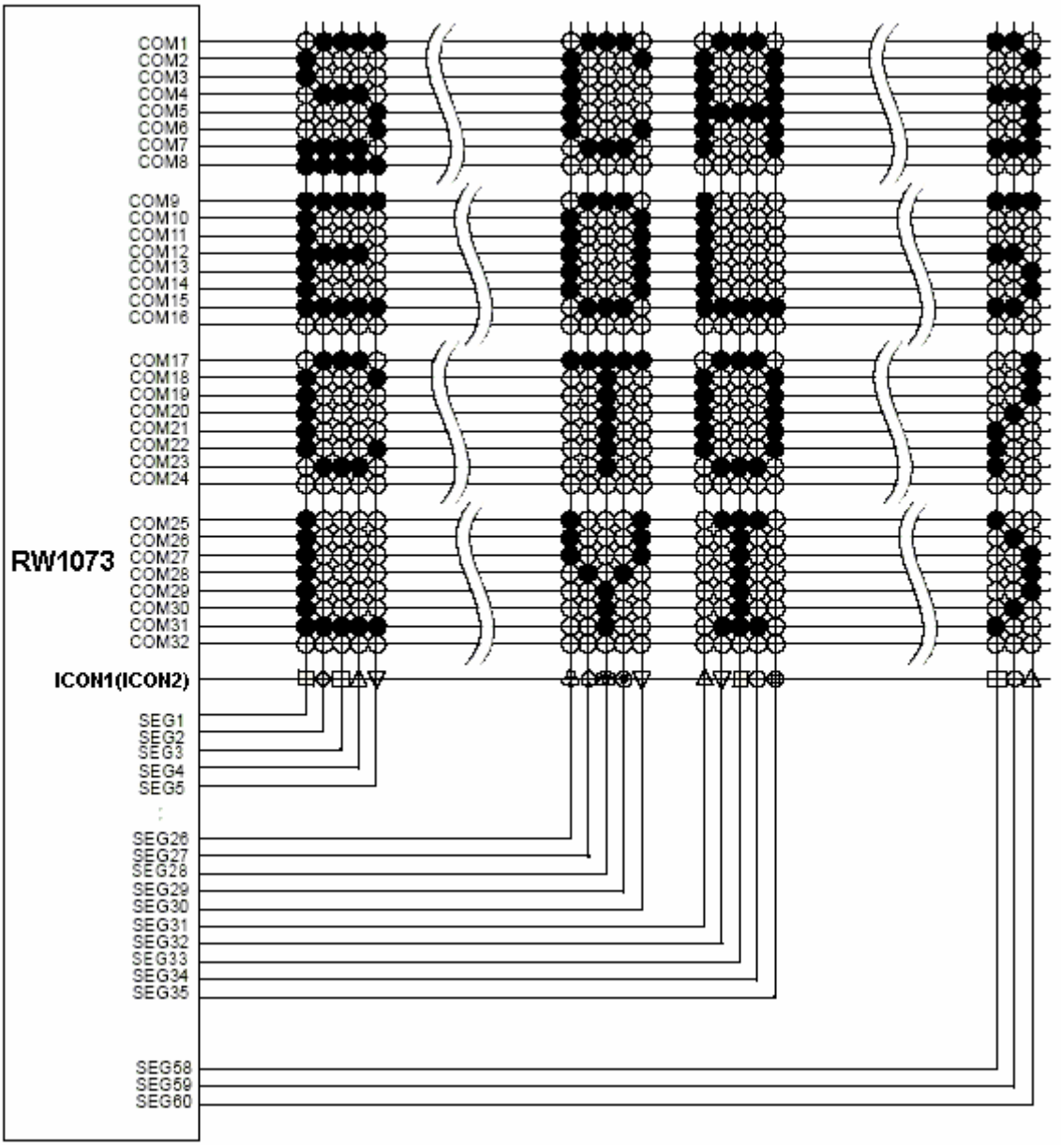
1) LCD Panel: 24 characters × 1-line format (5-dot font, 1/17 duty)



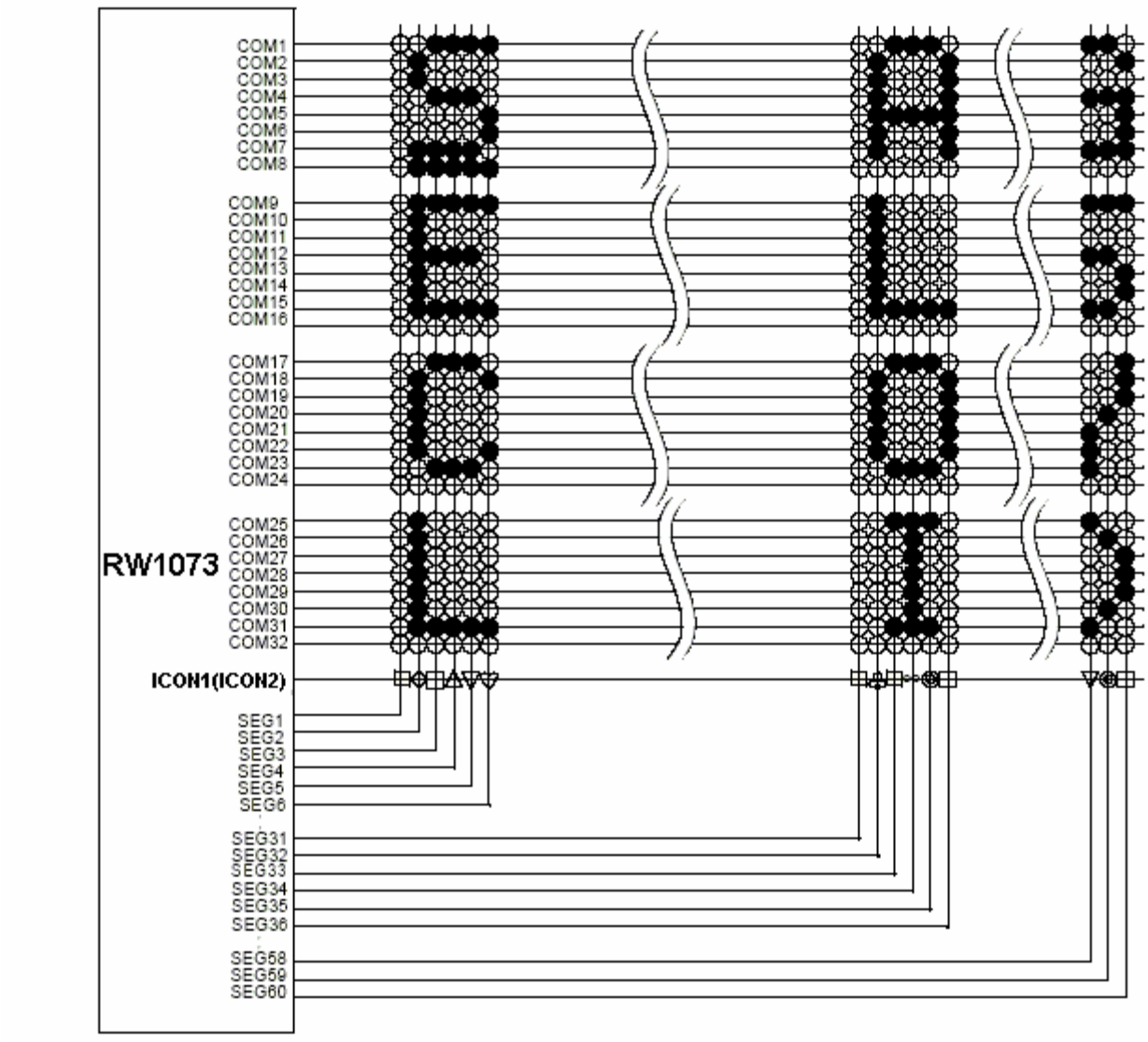
2) LCD Panel: 24 character × 2-line format (5-dot font, 1/33 duty)



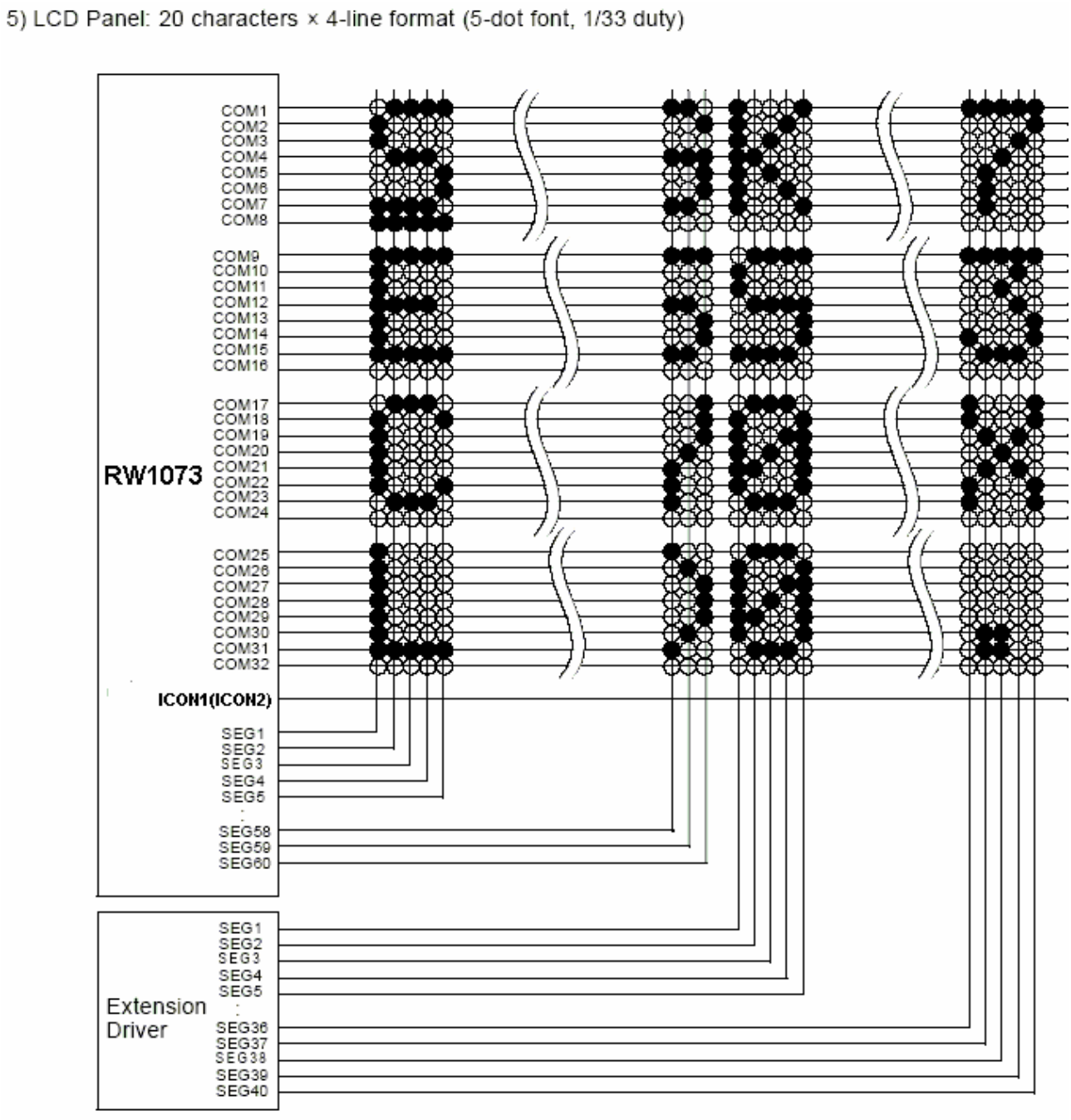
3) LCD Panel: 12 character × 4-line format (5-dot font, 1/33 duty)



4) LCD Panel: 10 characters × 4-line format (6-dot font, 1/33 duty)



5) LCD Panel: 20 characters × 4-line format (5-dot font, 1/33 duty)



■ INITIALIZING

1) Initializing by Internal Reset Circuit

When the power is turned on, RW1073 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High"(busy state) to the end of initialization.

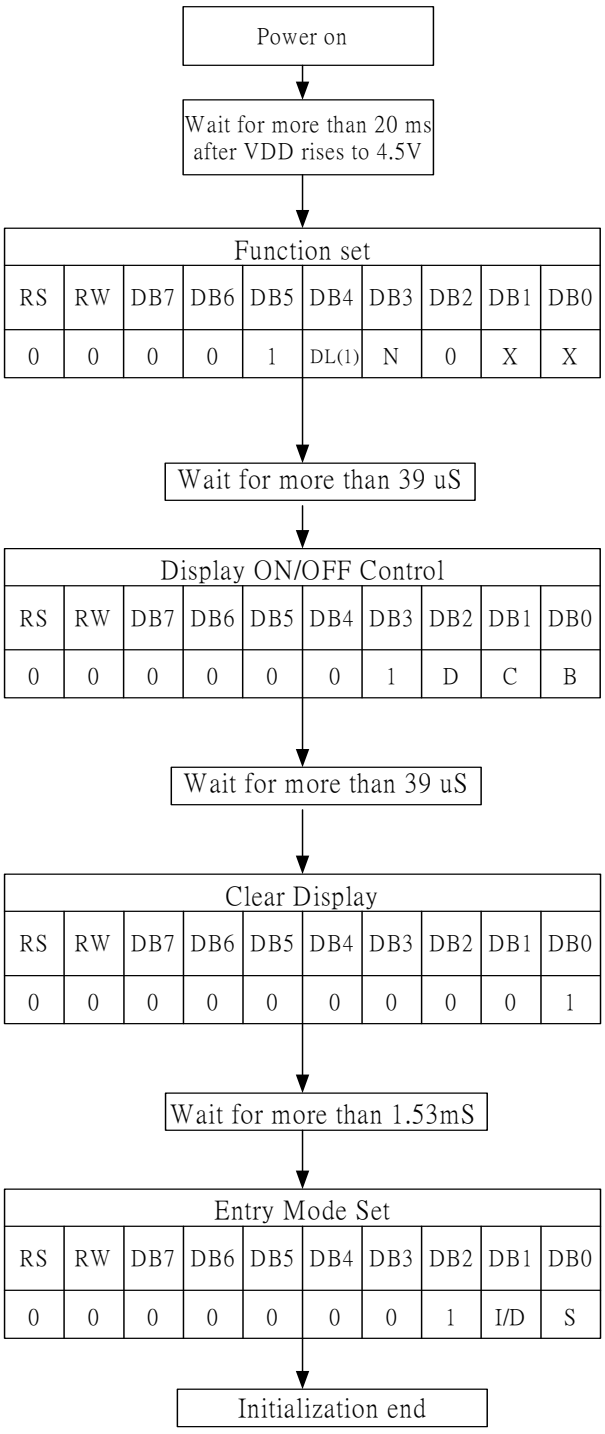
(1) Clear Display instruction Write "20H" to all DDRAM
(2) Functions Set instruction
DL = 1: 8-bit bus mode
N = 1: 2-line display mode
RE = 0: Extension register disable
BE = 0: CGRAM/SEGRAM blink OFF
DH = 0: display shift disable
REV = 0: Normal display mode (Not reversed display)
(3) Display ON/OFF Control instruction
D = 0: Display OFF, C = 0: Cursor OFF, B = 0: Blink OFF
(4) Entry Mode set instruction
I/D = 1: Increment by 1
S = 0: No entire display shift
BID = 0: Normal direction segment port
(5) Extension Function Set instruction
FW = 0: 5-dot font width character display
B/W = 0: Normal cursor (8th line)
NW = 0: Not 4-line display mode, 2-line mode is set because of N ("1")
(6)Shift Enable instruction
DS = 0000: Shift per line disable.

2) Initializing by Hardware RESET input

When RESET pin = "Low", RW1073 can be initialized as in the case of power on reset. During the power on reset operation, this pin is ignored.

■ INITIALIZING BY INSTRUCTION

(1)8-bit interface mode



Condition: fosc= 270KHz

DL	0	4-bit interface
	1	8-bit interface

N	0	1-line mode
	1	2-line mode

D	0	Display off
	1	Display on

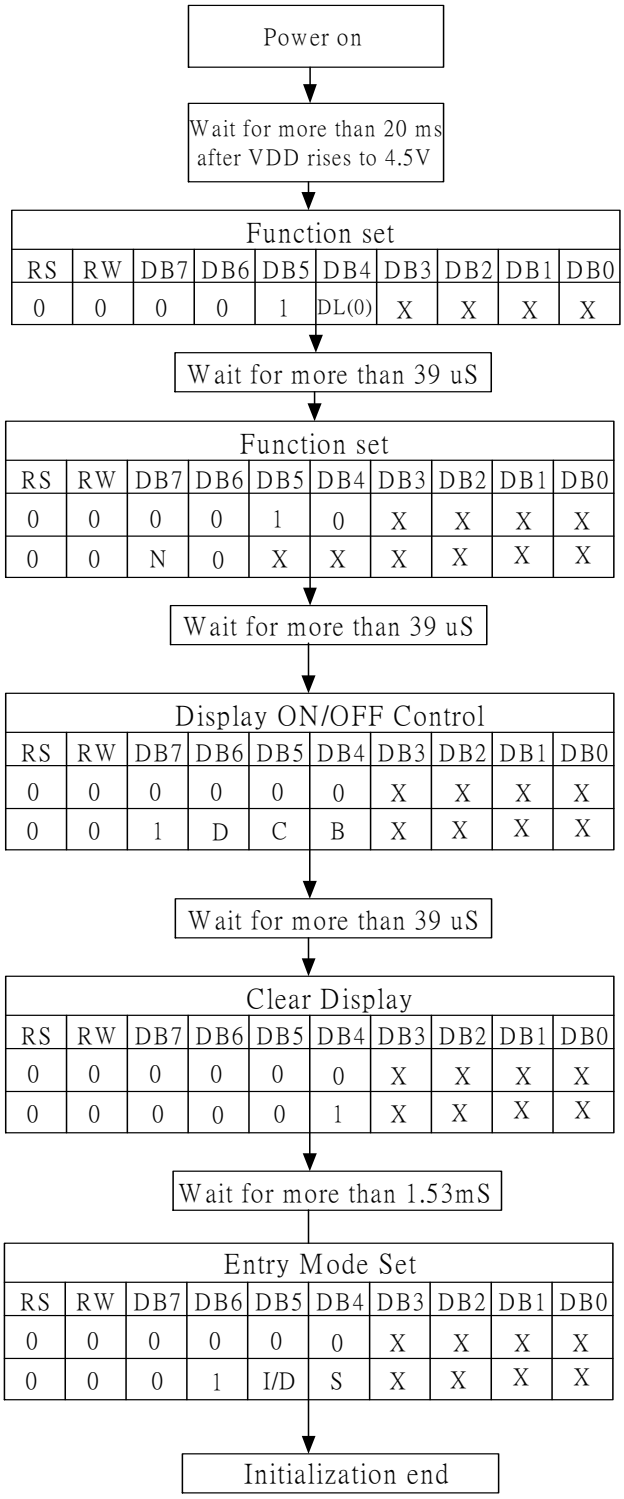
C	0	Cursor off
	1	Cursor on

B	0	Blink off
	1	Blink on

I/D	0	decrement mode
	1	increment mode

S	0	entire shift off
	1	entire shift on

(2)4-bit interface mode



Condition: fosc= 270KHz

DL	0	4-bit interface
	1	8-bit interface

N	0	1-line mode
	1	2-line mode

D	0	Display off
	1	Display on

C	0	Cursor off
	1	Cursor on

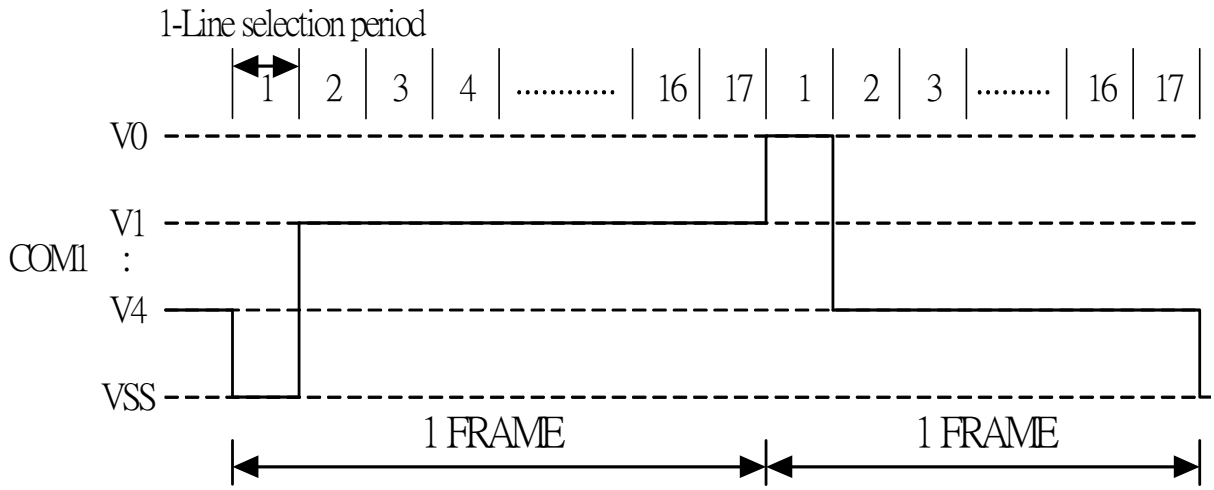
B	0	Blink off
	1	Blink on

I/D	0	decrement mode
	1	increment mode

S	0	entire shift off
	1	entire shift on

■ FRAME FREQUENCY

(1) 1/17 Duty Cycle

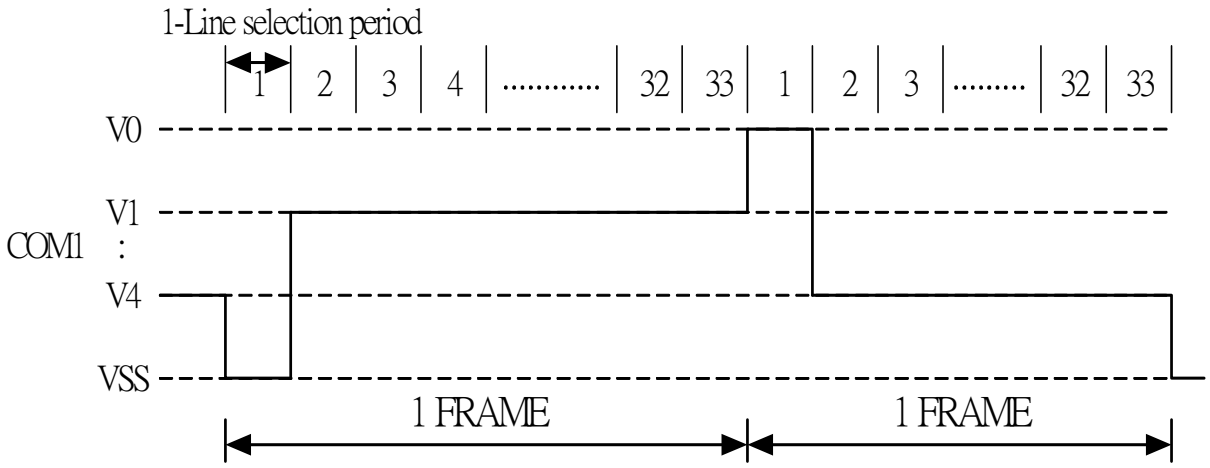


VDD=5V

Item	Normal Display Mode	
	5-dot width	6-dot width
1-line selection period	200 clocks	240 clocks
Frame frequency	79.4 Hz	66.2 Hz

***fosc= 270 Khz (1 clock=3.7uS)**

(1) 1/33 Duty Cycle



VDD=5V

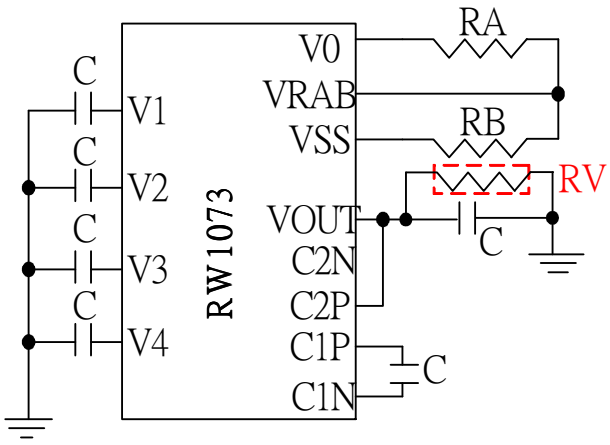
Item	Normal Display Mode	
	5-dot width	6-dot width
1-line selection period	100 clocks	120 clocks
Frame frequency	81.8 Hz	68.2 Hz

***fosc= 270 Khz (1 clock=3.7uS)**

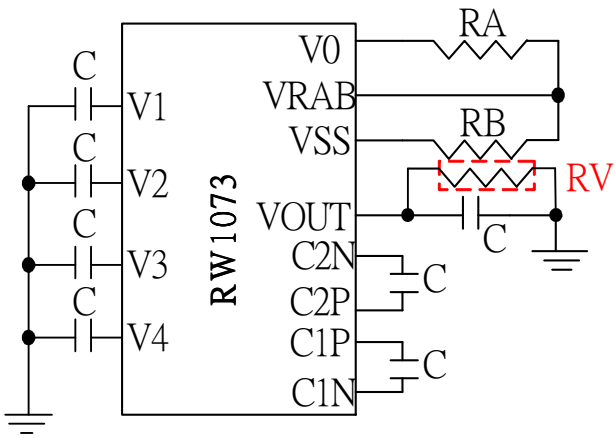
■ POWER SUPPLY FOR DRIVING LCD PANEL

◆ Booster Circuit:

Booster efficiency is around 80%
When VDD=5V, select 2-time booster, VOUT voltage is around 10V*0.8=8V
When VDD=3.3V, select 3-time booster, VOUT voltage is around 10V*0.8=7.9V
VOUT voltage 8V Max (2-time/3-time)



Use 2-time booster

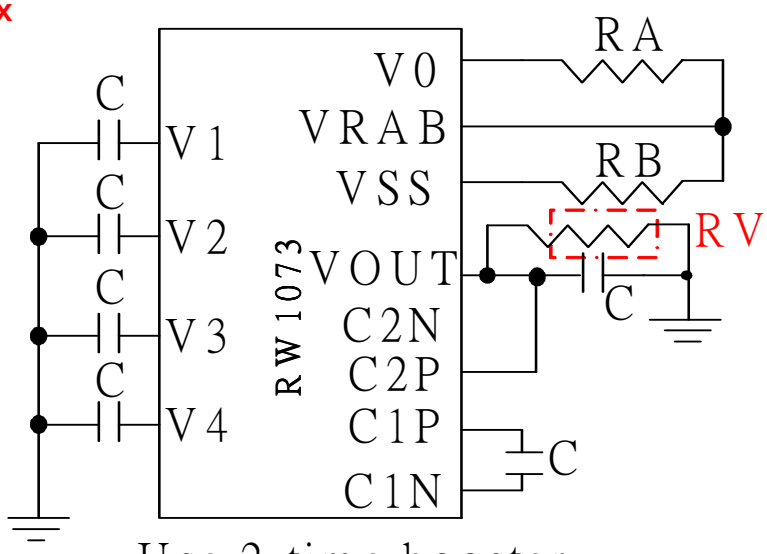


Use 3-time booster

RV resistor is protection and discharge resistor:
RV resistor use: 200K ohms.

◆ V0 Circuit: (FOFF=VDD)

V0 voltage 7.2V Max

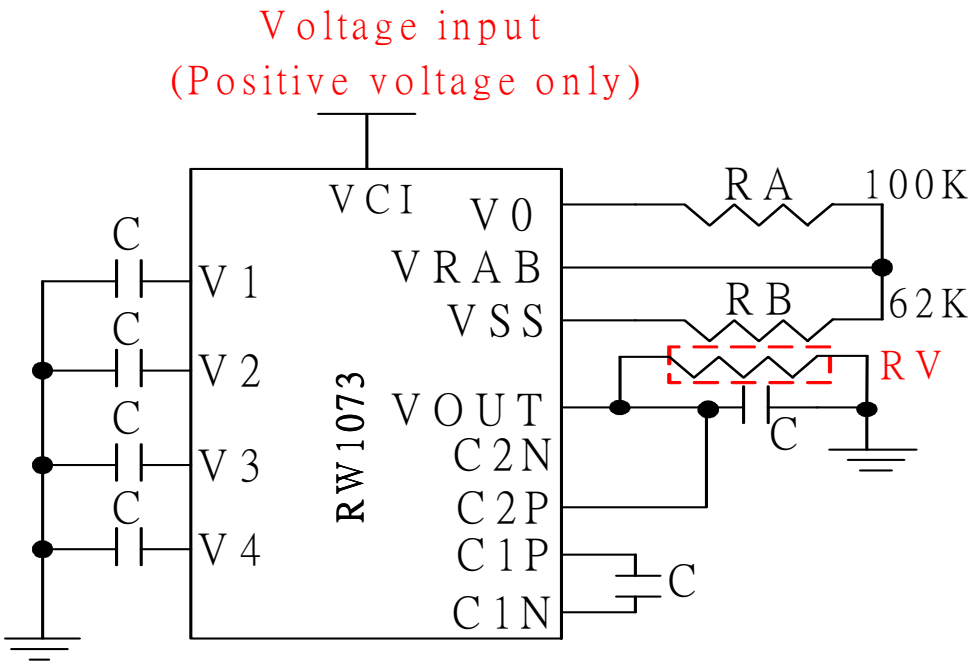


Use 2-time booster

V0=((VDD*0.5)/RB)*(RA+RB)

◆ **VCI Input Voltage Circuit (FOFF=VSS)**

VCI input voltage just can positive voltage only
V0 voltage 7.2V Max



$$V0=((VCI/RB)*(RA+RB))$$

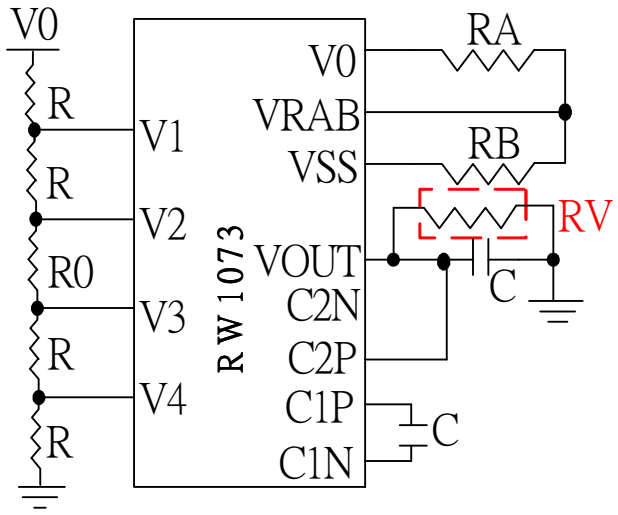
RV resistor is protection and discharge resistor:
RV resistor use: 200K ohms

Ex: When VDD=5V, 2X, RA=100K, RB=62K, external VCI voltage input

VCI voltage input	V0 output Voltage
1.0V	3.4V
1.1V	3.5V
:	:
:	:
1.9V	6.5V
2.0V	6.8V
2.1V	7.2V

◆ **When an external bias used (FOFF=VDD)**

(a)Use internal V0 and VOUT circuit, external bias circuit
R: 5.1K ohm RV: 1M~1.5M ohms



(b)External bias circuit: C1N/P, C2N/P, VOUT, V0, VRAB is floating
R: 5.1K ohm

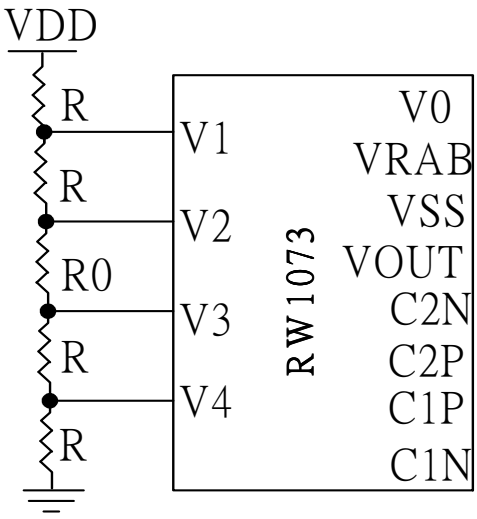


Table13. Duty Ratio and Power Supply for LCD Driving

Item		Data	
Number of lines		1	2 and 4
Duty ratio		1/17	1/33
Bias		1/6.7	1/6.7
Divided resistance	R	R	R
	R0	2.7*R	2.7*R

■ Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{CC}	-0.3 to +5.5
LCD Driver Voltage	V_{LCD}	Vss+7.2 to Vss-0.3
Input Voltage	V_{IN}	-0.3 to Vcc+0.3
Operating Temperature	T_A	-30°C to + 85°C
Storage Temperature	T_{STO}	-55°C to + 125°C

* Voltage greater than above may do damage to the circuit (V0, V1, V2, V3, V4, VSS)

■ DC Characteristics

(TA = 25℃ , VCC = 2.7 V - 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VCC	Operating Voltage	-	2.7	-	4.5	V
VLCD	LCD Voltage	V0-VSS	3.0	-	7.2	V
IDD	Power Supply Voltage	Fosc=270KHz Vcc=3.0V	-	0.25	0.6	mA
VIH1	Input High Voltage(Except OSC1)	-	0.7Vcc	-	Vcc	V
VIL1	Input Low Voltage (Except OSC1)	-	-0.3	-	0.6	V
VIH2	Input High Voltage(OSC1)	-	0.7Vcc	-	Vcc	V
VIL2	Input Low Voltage(OSC1)	-	-	-	0.2Vcc	V
VOH1	Output High Voltage(DB0~DB7)	IOH=-0.1mA	0.75Vcc	-	-	V
VOL1	Output Low Voltage(DB0~DB7)	IOL=-0.1mA	-	-	0.2Vcc	V
VOH2	Output High Voltage(Except DB0~DB7)	IOH=-0.04mA	0.8Vcc	-	Vcc	V
VOL2	Output Low Voltage(Except DB0~DB7)	IOL=-0.04mA	-	-	0.2Vcc	V
RCOM	Common Resistance (Sink)	VLCD=4V, Id=0.05mA	-	1.5	30	KΩ
RSEG	Segment Resistance (Sink)	VLCD=4V, Id=0.05mA	-	1.5	30	KΩ
ILEAK	Input Leakage	VIN=0Vto VCC	-1	-	1	uA
IPUP	Pull Up Mos Current	VCC=3V	10	50	120	uA

(TA = 25℃ , VCC = 4.5 V - 5.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VCC	Operating Voltage	-	4.5	-	5.5	V
VLCD	LCD Voltage	V0-VSS	3.0	-	7.2	V
IDD	Power Supply Voltage	Fosc=270KHz Vcc=5.0V	-	0.33	0.7	mA
VIH1	Input High Voltage(Except OSC1)	-	2.5	-	VCC	V
VIL1	Input Low Voltage (Except OSC1)	-	-0.3	-	0.6	V
VIH2	Input High Voltage(OSC1)	-	Vcc-1	-	VCC	V
VIL2	Input Low Voltage(OSC1)	-	-	-	1.0	V
VOH1	Output High Voltage(DB0~DB7)	IOH=-0.1mA	3.9	-	VCC	V
VOL1	Output Low Voltage(DB0~DB7)	IOL=-0.1mA	-	-	0.4	V
VOH2	Output High Voltage(Except DB0~DB7)	IOH=-0.04mA	0.9VCC	-	VCC	V
VOL2	Output Low Voltage(Except DB0~DB7)	IOL=-0.04mA	-	-	0.1VCC	V
RCOM	Common Resistance (Sink)	VLCD=4V, Id=0.05mA	-	1.5	20	KΩ
RSEG	Segment Resistance (Sink)	VLCD=4V, Id=0.05mA	-	1.5	30	KΩ
ILEAK	Input Leakage	VIN=0Vto VCC	-1	-	1	uA
IPUP	Pull Up Mos Current	VCC=5V	90	200	330	uA

■ AC Characteristics

(V_{DD} = 4.5 to 5.5V, Ta = -30 to +85 °C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(1) Write Mode (Refer to Fig-21)	E Cycle Tim	tc	500	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	th1	10	-	-	
	Data Setup Time	tsu2	60	-	-	
	Data Hold Time	th2	10	-	-	
(2) Read Mode (Refer to Fig-22)	E Cycle Tim	tc	500	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	th	10	-	-	
	Data Output Delay Tim	t_D	-	-	160	
	Data Hold Time	t_{DH}	5	-	-	
(3) Serial Interface Mod (Refer to Fig-23)	Serial Clock Cycle Time	tc	0.5	-	20	s
	Serial Clock Rise/Fall Time	tr,tf	-	-	50	ns
	Serial Clock Width (High, Low)	tw	200	-	-	
	Chip Select Setup Time	tsu1	60	-	-	
	Chip Select Hold Time	th1	20	-	-	
	Serial Input Data Setup Tim	tsu2	100	-	-	
	Serial Input Data Hold Time	th2	100	-	-	
	Serial Output Data Delay Time	t_D	-	-	160	
	Serial Output Data Hold Time	t_{DH}	5	-	-	

(V_{DD} = 2.7 to 4.5V, Ta = -30 to +85 °C)

Mode	Item	Symbol	Min	Type	Max	Unit
(4) Write Mode (Refer to Fig-21)	E Cycle Tim	tc	100	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	th1	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	th2	10	-	-	
(5) Read Mode (Refer to Fig-22)	E Cycle Tim	tc	100	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	th	20	-	-	
	Data Output Delay Tim	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	
(6) Serial Interface Mod (Refer to Fig-23)	Serial Clock Cycle Time	tc	1	-	20	s
	Serial Clock Rise/Fall Time	tr,tf	-	-	50	ns
	Serial Clock Width (High, Low)	tw	400	-	-	
	Chip Select Setup Time	tsu1	60	-	-	
	Chip Select Hold Time	th1	20	-	-	
	Serial Input Data Setup Tim	tsu2	200	-	-	
	Serial Input Data Hold Time	th2	200	-	-	
	Serial Output Data Delay Time	t_D	-	-	360	
	Serial Output Data Hold Time	t_{DH}	5	-	-	

(V_{DD} = 2.7 to 4.5V, Ta = -30 to +85 °C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(7) Interface Mode with Extension Driver (Refer to Fig-24)	Clock Pulse Width (High, Low)	tw	800	-	-	ns
	Clock Rise / Fall Time	tr,tf	-	-	100	
	Clock Setup Tim	tsu1	500	-	-	
	Data Setup Time	tsu2	300	-	-	
	Data Hold Time	t_{DH}	300	-	-	
	M Delay Time	t_{DM}	-1000	-	1000	

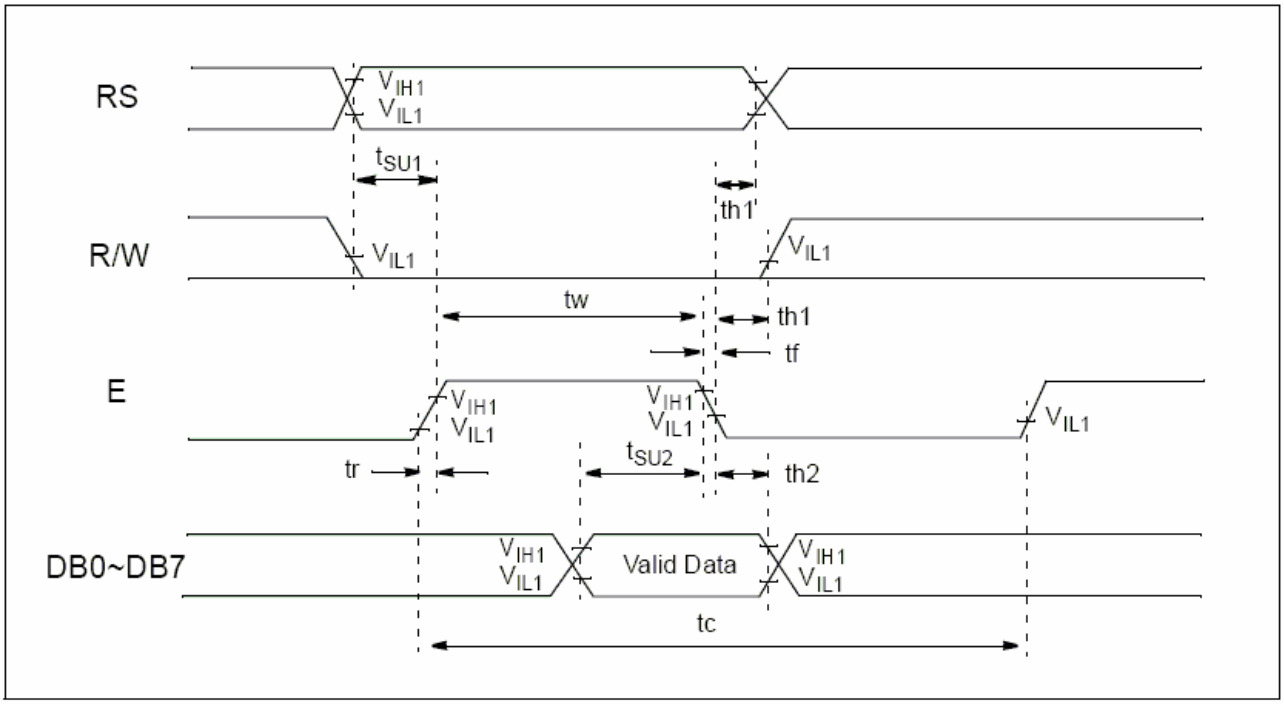


Fig-21. Write Mode

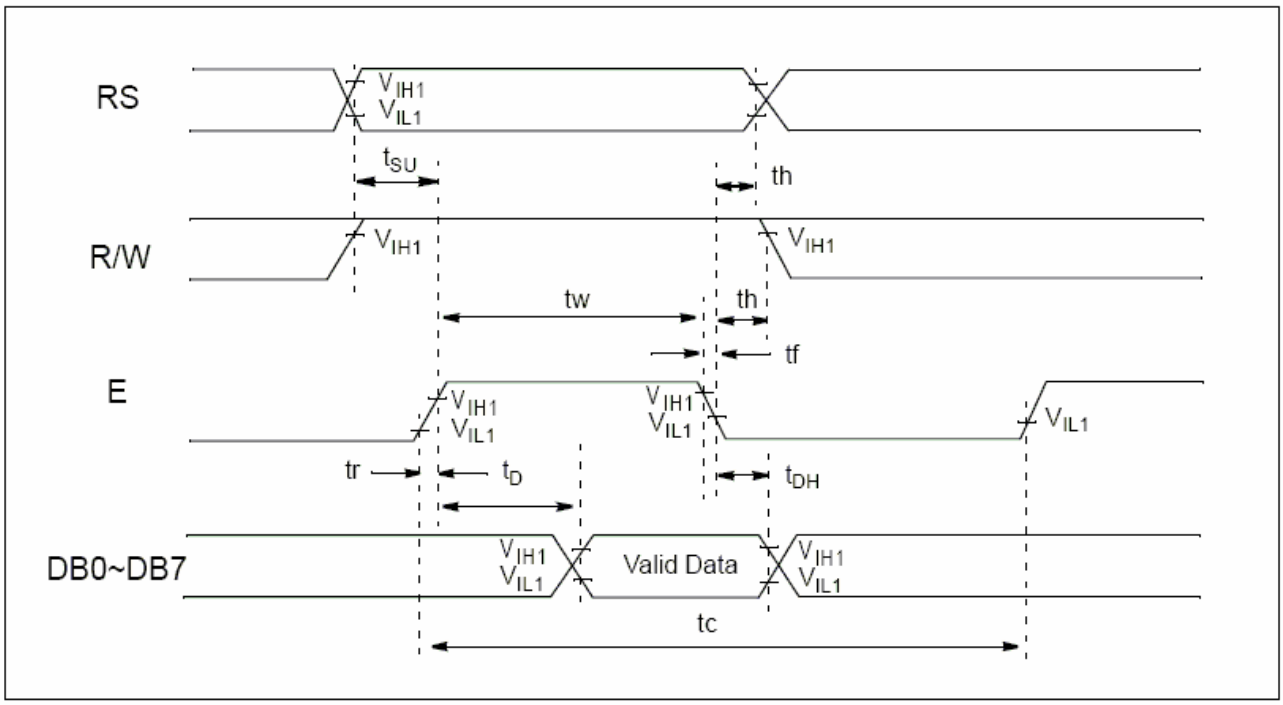


Fig-22. Read Mod

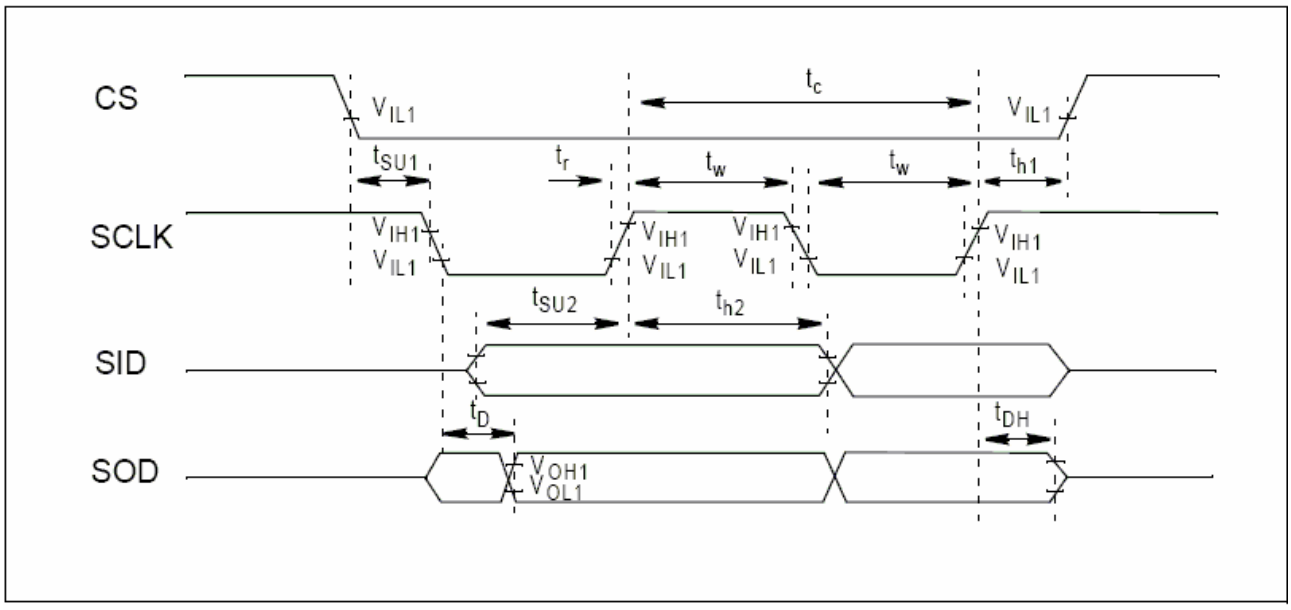


Fig-23. Serial Interface Mode

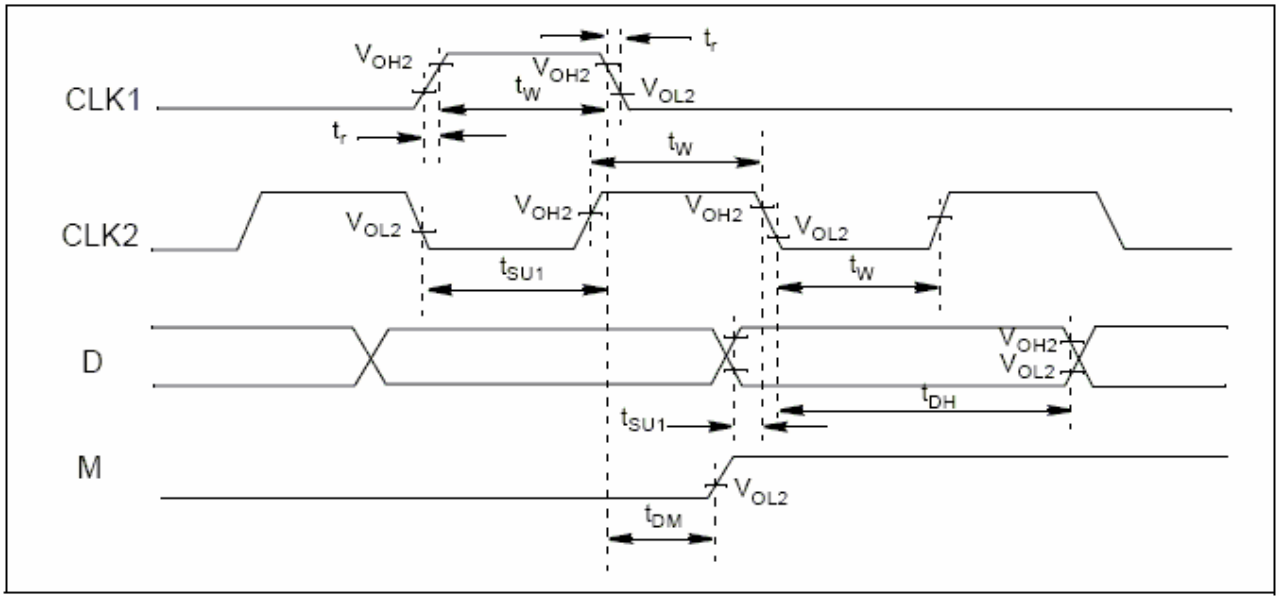


Fig-24. Interface Mode with Extensive Driver

■ RESET TIMING

(V_{DD} = 2.7 to 5.5V, Ta = -30 to +85 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Reset Low level width (Refer to Fig-25)	tRES	1	-	-	ms

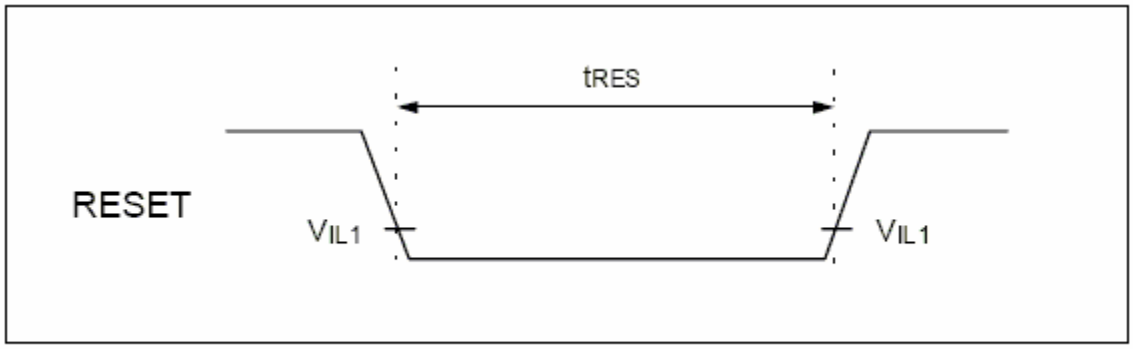


Fig-25. Reset TimingDiagram

RW1073 Code Bank (0B-002)